

## 1 GENERAL DESCRIPTION

The CCG1401 is a universal programmable amplifier for optical sensor applications. The chip can be delivered in a QFN16 package or as a Chip Size Package (CSP) for very small PCB footprints.

### 1.1 FEATURES

- Universal amplifier for optical sensor applications
- Programmable transimpedance
- Programmable upper frequency range
- Programmable threshold voltages
- Single supply voltage
- Low current consumption
- Standby mode

### 1.2 SCHEMATIC

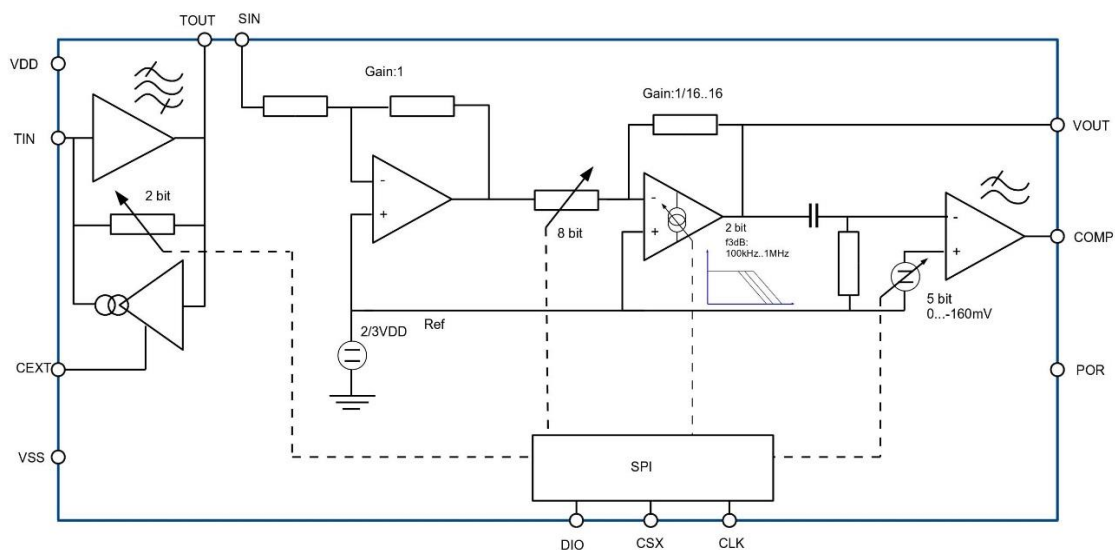


Figure 1 – CCG1401 Block Diagram

## 2 PINOUT

### 2.1 PACKAGE QFN16

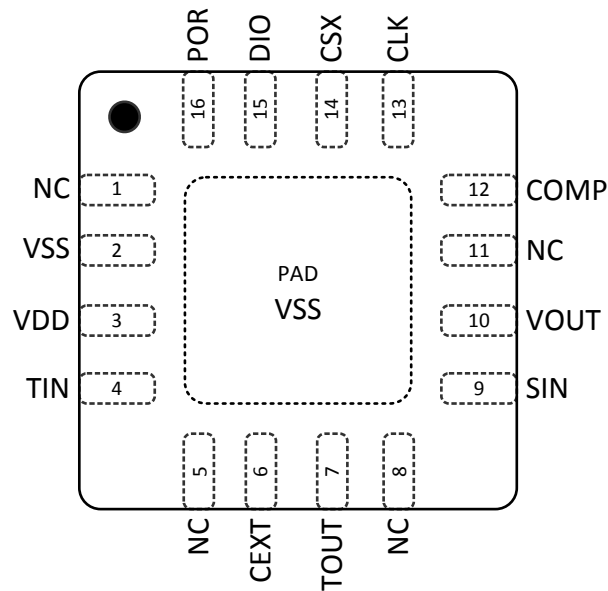


Figure 2 - CCG1401 - QFN16 (Top View)

### 2.2 CHIP SIZE PACKAGE

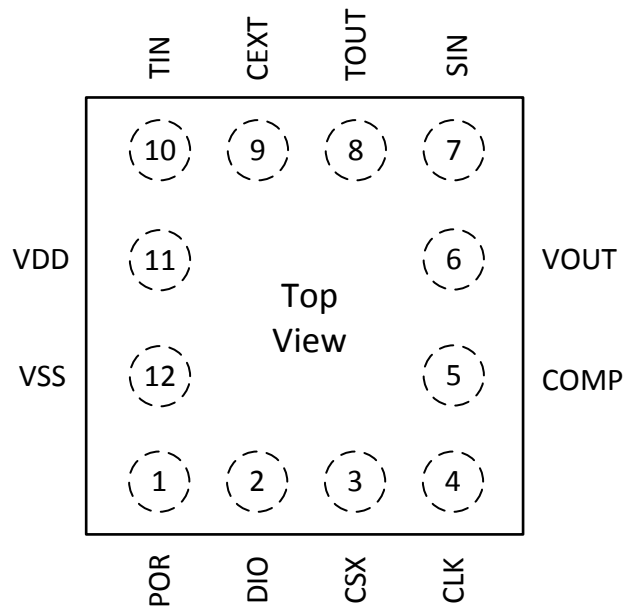


Figure 3 - CCG1401 Pad configuration (CSP/Bumped Die)

## 2.3 PIN DESCRIPTIONS

Pin no. QFN16	Pin.no. CSP	Name	Type	Function
1	-	NC	-	Not connected
2	12	VSS	PWR	Signal/PWR Ground
3	11	VDD	PWR	Power Supply
4	10	TIN	IN	Input TIA
5	-	NC	-	Not connected
6	9	CEXT	IN	External Capacitor TIA
7	8	TOUT	OUT	Output TIA
8	-	NC	-	Not connected
9	7	SIN	IN	Input SUM Amplifier
10	6	VOUT	OUT	Analog Output
11	-	NC	-	Not connected
12	5	COMP	OUT	Comparator Output
13	4	CLK	IN	Serial Interface CLOCK
14	3	CSX	IN	Serial Interface ENABLE
15	2	DIO	IN/OUT	Serial Interface DATA IN/OUT
16	1	POR	OUT	Power-ON Reset Output

Table 1 - CCG1401 Pin Descriptions

## 3 ABSOLUTE MAXIMUM RATINGS

Absolute maximum ratings are allowed for short periods of time only, otherwise product reliability degrades.

Parameter	Symbol	Conditions	Min.	Max.	Unit
Supply voltage	$V_{DD}$		-0,60	6	V
Total power dissipation	$P_{TOT}$	@ $\vartheta_{op}=125\text{ }^{\circ}\text{C}$		20	mW
Storage temperature range	$\vartheta_{storage}$		-55	150	$^{\circ}\text{C}$
Soldering profile	$t_{soldering}$	$\vartheta_{sol\_max}=260\text{ }^{\circ}\text{C}$		12	s
ESD protection	$V_{ESD}$	Human Body model ESDA/JEDEC – JS-001-2014	2		kV
Permanent current into ESD protection diodes	$I_{DC\_ESD}$	Only in case of forward biased ESD diodes. Input voltage above $V_{DD}$ or below $V_{SS}$		4	mA
Reliability	MTBF	@ $\vartheta_{amb}=27\text{ }^{\circ}\text{C}$		100	FIT

Table 2 - Absolute Maximum Ratings

## 4 ELECTRICAL CHARACTERISTICS

Electrical characteristics are valid for typical operating conditions, the whole specified operating temperature and supply voltage range unless otherwise specified.

### 4.1 GENERAL PARAMETERS

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Operating temperature range	$\vartheta_{op}$	Ambient temperature	-40		125	°C
Junction temperature range	$\vartheta_{j,op}$	Junction temperature	-40		130	°C
Input capacitance	$C_{ID}$	Maximum capacitance of connected photodiode			150	pF
Coupling capacitor between TOUT and SIN	$C_{int}$	Typical values are recommended. Change in value could lead to change in absolute transimpedance and bandwidth.		0.32		nF
External capacitor @ CEXT <sup>1</sup> to Ground	$C_{ext}$	Smaller than minimum values can lead to peaking, should be avoided. Higher than typical values will change bandwidth and transimpedance value.	2	5		nF
Load resistance at COMP	$R_{Load\_COMP}$		10			kΩ
Load capacitance at COMP	$C_{Load\_COMP}$				200	pF
Load resistance at VOUT	$R_{Load\_VOUT}$		4.7			kΩ
Load capacitance at VOUT	$C_{Load\_VOUT}$				100	pF

Table 3 - General Parameters

Note 1: The transimpedance amplifier has a bandpass characteristic dependent from the external capacitor  $C_{ext}$  and operating condition. The low bandpass cut-off frequency can be calculated as follows:

$$f_c = \frac{1}{2 * \pi * I_{DC,in}^{-(K*\ln(M)+0.06)} * 1800 * M^{Exp} * C_{ext}}$$

With:

- $I_{DC,in}$  Transimpedance amplifier input current (formula valid range 1μA to specified max value, see 4.3. Transimpedance Input Stage)
- K Input current exponent = 0.14
- M Transimpedance control variable
- Exp Control variable exponent = -1.2
- $C_{ext}$  External capacitor

## 4.2 POWER SUPPLY

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Supply voltage	V <sub>DD</sub>		3		5.5	V
Current consumption	I <sub>DD</sub>	V <sub>DD</sub> =5.5V, no external load currents		2.5	3	mA
Standby current	I <sub>DDstandby</sub>	no external load currents, CSX=CLK=High			15	μA

Table 4 - Power Supply

## 4.3 TRANSIMPEDANCE INPUT STAGE / BANDWIDTH LIMITATION

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Transimpedance control	M	Adjustable in three steps: 1, 8, 64	1	8	64	
Transimpedance ratio tolerance	ΔM/M	Deviation of ratio from step to step; I <sub>DC_IN</sub> =3μA		3	11	%
Transimpedance	R <sub>T3</sub>	M=64, T=27°C, f <sub>meas</sub> =100kHz		210		kΩ
	R <sub>T2</sub>	M=8, T=27°C, f <sub>meas</sub> =100kHz		26		kΩ
	R <sub>T1</sub>	M=1, T=27°C, f <sub>meas</sub> =100kHz		3.3		kΩ
Tolerance of transimpedance	ΔR <sub>T</sub> /R <sub>T</sub>	M=1, 8, 64; T=27°C	-30		30	%
Temperature coefficient	TC <sub>RT</sub>			700	900	ppm/K
Tolerance of transimpedance over I <sub>DC_IN</sub>	ΔR <sub>T</sub> /R <sub>T_IDC</sub>	M=64 I <sub>DC_IN</sub> =0.1μA...100μA			5	%
Transimpedance V <sub>DD</sub> drift	ΔR <sub>T</sub> /R <sub>T_VDD</sub>	M=1, 8, 64 3≤V <sub>DD</sub> ≤3.3V 3.3≤V <sub>DD</sub> ≤5.5V			6 1	%
Input resistance	R <sub>L_TIA</sub>	Load TOUT: C=320pF and R=10kΩ in series to ground			1.7	kΩ
DC input current @ TIN	I <sub>DC_IN</sub>	M=64			100	μA
		M=8			800	μA
		M=1			1500	μA
Input noise current	I <sub>NOISE</sub>	200 kHz noise bandwidth, 6 dB SNR @ I <sub>DC_IN</sub> =1μA			2.5	pA/√Hz

Table 5 - Transimpedance Input Stage / Bandwidth Limitation

## 4.4 PROGRAMMABLE AMPLIFIER / ANALOG OUTPUT

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input resistance	R <sub>L_AMP</sub>		7	10	13	kΩ
Gain control resolution	GA			8		BIT
Gain control range	Gain	GA=0 minimum value		1/16		
		GA=15		1		
		GA=255 maximum value		16		
3dB cut-off frequency control	f <sub>AMP_3dB</sub>	GA=255, GFA=0		100		kHz
		GA=255, GFA=1		250		kHz
		GA=255, GFA=2		500		kHz
		GA=255, GFA=3		1000		kHz
Output voltage	V <sub>OUT</sub>	R <sub>Load_VOUT</sub> =4.7 kΩ	0.2		4.8	V
DC output voltage	V <sub>OUT_DC</sub>			2/3 V <sub>DD</sub>		

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Output slew rate	SR <sub>out</sub>	3V step at pin SIN, C <sub>Load_VOUT</sub> =100pF, V <sub>DD</sub> =3V GA=15, GFA=0	[0.3]			V/μs
		3V step at pin SIN, C <sub>Load_VOUT</sub> =100pF, V <sub>DD</sub> =3V GA=15, GFA=1	[0.6]			V/μs
		3V step at pin SIN, C <sub>Load_VOUT</sub> =100pF, V <sub>DD</sub> =3V GA=15, GFA=2	[1.2]			V/μs
		3V step at pin SIN, C <sub>Load_VOUT</sub> =100pF, V <sub>DD</sub> =3V GA=15, GFA=3	[2.4]			V/μs

Table 6 - Programmable Amplifier / Analog output

## 4.5 COMPARATOR

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Input offset voltage	V <sub>offs</sub>	3σ			±8	mV
Noise filter gate time	t <sub>NOISE_GATE</sub>	Toggle input voltage over threshold, comparator output doesn't reach 0.7V	80			ns
Low limit threshold voltage	V <sub>SREF</sub>	referenced to 2/3 V <sub>DD</sub> , G <sub>SREF</sub> =31	-186			mV
Upper limit threshold voltage		referenced to 2/3 V <sub>DD</sub> , G <sub>SREF</sub> =0			28	
Threshold voltage deviations	ΔV <sub>SREF</sub>	G <sub>SREF</sub> =0...31			±28	mV
Threshold voltage resolution	G <sub>SREF</sub>	Linear steps		5		BIT
Threshold voltage step size	V <sub>SREF_step</sub>			5.1		mV
Settling time V <sub>SREF</sub>	t <sub>settling</sub>	After asserting CSX signal (low->high; SPI communication cycle)			10	μs

Table 7 - Comparator

## 4.6 OVERALL SYSTEM DATA

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Total transimpedance (V <sub>out</sub> / I <sub>foto</sub> )	R <sub>TT</sub>	M=64, Gain=1/16 @ f <sub>meas</sub> =100kHz	8.5			kΩ
		M=64, Gain=16 @ f <sub>meas</sub> =100kHz			3500	
		M=8, Gain=1/16 @ f <sub>meas</sub> =100kHz	1.0			
		M=8, Gain=16 @ f <sub>meas</sub> =100kHz			430	
		M=1, Gain=1/16 @ f <sub>meas</sub> =100kHz	0.145			
		M=1, Gain=16 @ f <sub>meas</sub> =100kHz			54.5	
Temperature coefficient R <sub>TT</sub>	TCR <sub>TT</sub>				600	ppm/K
Total transimpedance V <sub>DD</sub> drift	ΔR <sub>TT</sub> /R <sub>TT</sub>	M=1, 8, 64 3 ≤ V <sub>DD</sub> ≤ 3.3V 3.3 ≤ V <sub>DD</sub> ≤ 5.5V			2 1	%
Settling time after overdrive input T <sub>IN</sub>	t <sub>set</sub>	100 times overdrive, ΔV <sub>OUT,DC</sub> / V <sub>OUT,DC</sub> = 1% M=1, 8, 64, GA=15		30	55	μs
Bandlimiting frequency	f <sub>l</sub>	M=1, 8, 64	20		40	kHz
	f <sub>u</sub>		170		270	

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Low frequency suppression	a <sub>100</sub>	@100Hz	-50	-70		dB
Dead time between input and output response	t <sub>dead</sub>	V <sub>DD</sub> =5V, I <sub>DC_IN</sub> =10μA, G <sub>SREF</sub> =0, M=1, Pulse current=25μA Monitor pin V <sub>OUT</sub> t <sub>dead</sub> consists mainly of t <sub>prop</sub>		1.2	2.8	μs
Switching time from standby to operation	t <sub>sw_01</sub>	C <sub>ext</sub> = 5nF		150	200	μs
Switching time from operation to standby	t <sub>sw_10</sub>	C <sub>ext</sub> = 5nF			20	μs
Start-up time	t <sub>start</sub>	After reaching V <sub>DD</sub> =3V			2	ms

Table 8 - Overall System Data

## 4.7 POWER ON RESET

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power-on threshold	V <sub>POR_on</sub>	POR signal goes high @ V <sub>DD</sub> = V <sub>POR_on</sub>	2.4	2.6	2.8	V
Power-off threshold	V <sub>POR_off</sub>	POR signal goes low @ V <sub>DD</sub> = V <sub>POR_off</sub>	2.2	2.45	2.7	V
Hysteresis	V <sub>POR_hyst</sub>		100	160	230	mV

Table 9 – Power ON Reset

## 4.8 LOGIC OUTPUT COMP

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Low output voltage	V <sub>OL</sub>	I <sub>OUT</sub> =4mA, V <sub>DD</sub> =3...5V No input signal			0.8	V
High output voltage	V <sub>OH_5V</sub>	I <sub>OUT</sub> =-4mA, V <sub>DD</sub> =5V Signal detected	4.2			V
	V <sub>OH_3V</sub>	I <sub>OUT</sub> =-4mA, V <sub>DD</sub> =3V Signal detected	2.2			V
Slew rate	SR <sub>comp</sub>		25	50	90	V/μs
Propagation time	t <sub>prop</sub>			0.5	1.5	μs
Output leakage current	I <sub>O_LEAK</sub>		-0.5		0.5	μA

Table 10 - Logic Output COMP

## 4.9 LOGIC INPUT (DIO, CLK, CSX)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Low input voltage	V <sub>IL_3V</sub>	V <sub>DD</sub> =3.0V			0.5	V
	V <sub>IL_5V</sub>	V <sub>DD</sub> =5.0V			0.8	V
High input voltage	V <sub>IH_3V</sub>	V <sub>DD</sub> =3.0V	1.5			V
	V <sub>IH_5V</sub>	V <sub>DD</sub> =5.0V	2.2			V
Input capacitance	C <sub>in_d</sub>				40	pF
Frequency at CLK	f <sub>CLK</sub>				4	MHz

Table 11 - Logic Input (DIO, CLK, CSX)

## 5 FUNCTIONAL DESCRIPTION

### 5.1 SPI AND DIGITAL CONTROL

A synchronous serial interface receives data from an external controller via DIO, CLK and CSX. This interface consists of a 10 bit shift register, 2 bit header and 8 bit data. Each positive slope at CLK shifts the value at DIO into the shift register. With a positive slope at CSX the 8 databits of the shift register are transferred to the address register or a parameter register depending on the value of the header. A data package with header "00" selects a parameter register. Following data packages with header "01" are intended for the previously selected register.

To read out the registers content, the header needs to be "10". DIO changes then its functionality from input to output and DIO pin has to be released. Data can be shifted out with the positive edge of CLK. Sampling of data should occur on the negative edge. Maximum frequency when reading is 50 kHz. The output data starts with the register content at address 0, followed by the one at address 1 and ends with the content of register 4. After transfer of the last bit, when CSX goes high, DIO changes its functionality back to input behavior. The DIO-behavior is visualized by the internal signal DOUT\_EN in the timing diagram (see Figure 4).

Standby modus of analog circuitry can be selected by register (see 5.4.6) and alternatively by setting CSX=High and CLK=High. The SPI is not affected by standby operation.

The comparator threshold can be controlled by register content and setting DIO=High for using the register SREF1 (see 5.4.4) or setting DIO=Low for using register SREF2 (see 5.4.5). Take into consideration that this mechanism does not work during an SPI-transfer.

### 5.2 SPI TIMING

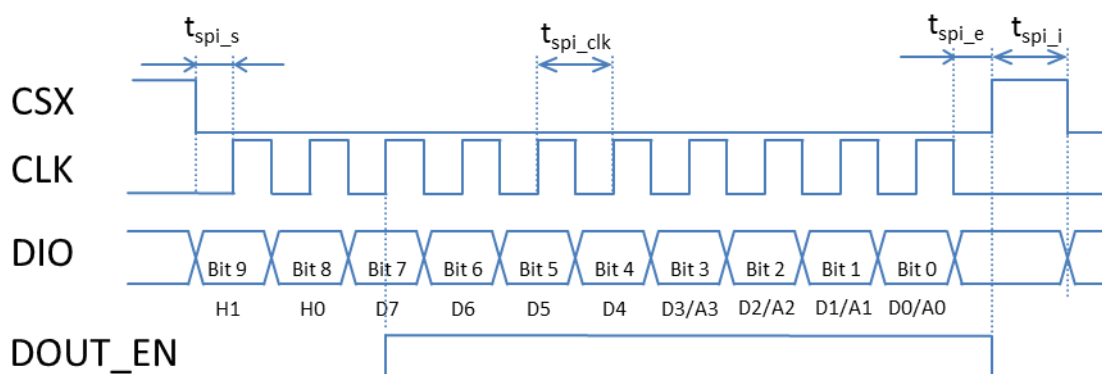


Figure 4 – Timing diagram

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SPI Clock Frequency	f <sub>SPI</sub>				4	MHz
SPI Clock Period	t <sub>SPI_CLK</sub>		250			ns
SPI Start Clock after Select	t <sub>SPI_S</sub>		125			ns
SPI End of Select after Clock	t <sub>SPI_E</sub>		125			ns
SPI Idle between Access	t <sub>SPI_I</sub>		250			ns

Table 12 - SPI Timing



After Power-on all register defaults are in logical state "High", except CIRC\_DIS in CTRL-register (see 5.4.6).

### 5.3 SPI PROTOCOL

10 bit shift register: 2 bit header, 8 bit address/data

Bit	9	8	7	6	5	4	3	2	1	0
Denotation	H1	H0	D7	D6	D5	D4	D3	D2	D1	D0
Message type 0 (SPI-Write address)	'0'	'0'	-	-	-	-	A3	A2	A1	A0
Message type 1 (SPI-Write data)	'0'	'1'	D7	D6	D5	D4	D3	D2	D1	D0
Message type 2 (SPI-Read data)	'1'	'0'	D7	D6	D5	D4	D3	D2	D1	D0

Table 13 - SPI Protocol

### 5.4 REGISTER DESCRIPTION

#### 5.4.1 Register Definitions

The register summary gives an overview of the available registers of the module.

Register address	Register name
0x0	TIA
0x1	GAIN
0x2	SREF1
0x3	SREF2
0x4	CTRL

Table 14 - Register Definitions

#### 5.4.2 TIA (Transimpedance Register)

Bit	7 : 2	1 : 0
Name	-	TI
Reset	0xFF	

Table 15 - TIA

Address: 0x0

*TI* Transimpedance range selector

- 0d: M=1
- 1d: M=8
- 2d: M=64
- 3d: default state, returns to M=64

#### 5.4.3 GAIN (Programmable Gain Register)

Bit	7 : 0
Name	GA
Reset	0xFF

Table 16 - GAIN

Address: 0x1

*GA Programmable amplifier gain adjustment*

$$\text{Gain} = (\text{GA} + 1) / 16$$

$$0\text{d: Gain} = 1 / 16$$

$$15\text{d: Gain} = 1$$

$$255\text{d: Gain} = 16 \text{ (default)}$$

#### 5.4.4 SREF1 (Programmable threshold voltage Register #1)

Bit	7 : 5	4 : 0
Name	-	SREF1
Reset	0xFF	

Table 17 – SREF1

Address: 0x2

*SREF1 Comparator threshold voltage 1*

Defines the comparator threshold voltage referenced to 2/3 VDD

$$V_{\text{sref}} \approx \text{SREF1} * -5.1\text{mV}$$

DIO = high

#### 5.4.5 SREF2 (Programmable threshold voltage Register #2)

Bit	7 : 5	4 : 0
Name	-	SREF2
Reset	0xFF	

Table 18 - SREF2

Address: 0x3

*SREF2 Comparator threshold voltage 2*

Defines the comparator threshold voltage referenced to 2/3 VDD

$$V_{\text{sref}} \approx \text{SREF2} * -5.1\text{mV}$$

DIO = low

#### 5.4.6 CTRL – General Control Register

Bit	7	6	5 : 2	1 : 0
Name	COMP_DIS	CIRC_DIS	-	GFA
Reset	0xBF (0b10111111)			

Table 19 - CTRL

Address: 0x4

*GFA Programmable summing amplifier 3dB frequency control adjustment*

$$0\text{d} \rightarrow \text{GFA} = 0$$

- 1d -> GFA=1
- 2d -> GFA=2
- 3d -> GFA=3

*CIRC\_DIS*      *Circuit disable (standby mode)*

- 0d -> circuit is enabled (This is the default value! Keep in mind that this is the only bit that is initialized with '0')
- 1d -> circuit is disabled

*COMP\_DIS*      *Comparator output disable*

- 0d -> comparator output is enabled
- 1d -> comparator output is disabled

## 6 APPLICATION NOTES

### 6.1 APPLICATION WITH PHOTODIODE SENSOR

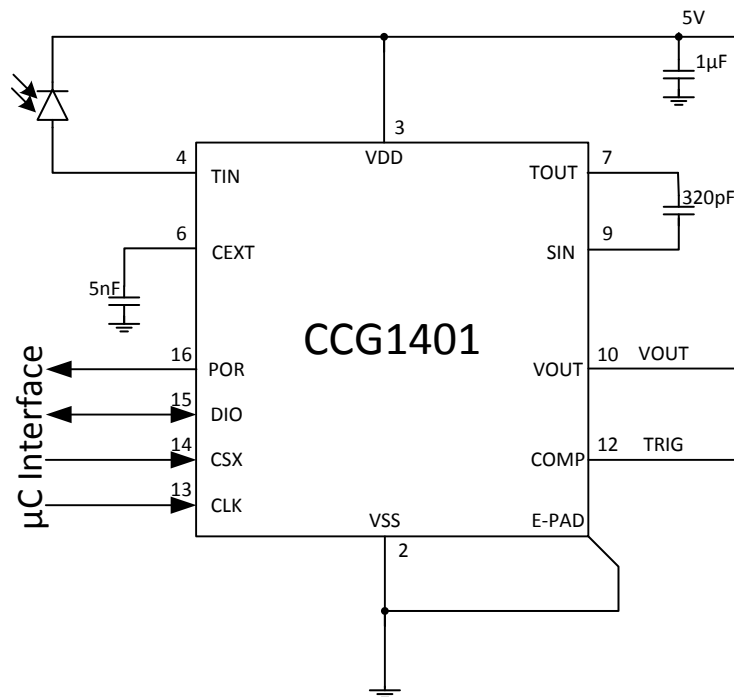


Figure 5 – Optical Application

## 7 PACKAGE OUTLINE

### 7.1 QFN16 PACKAGE

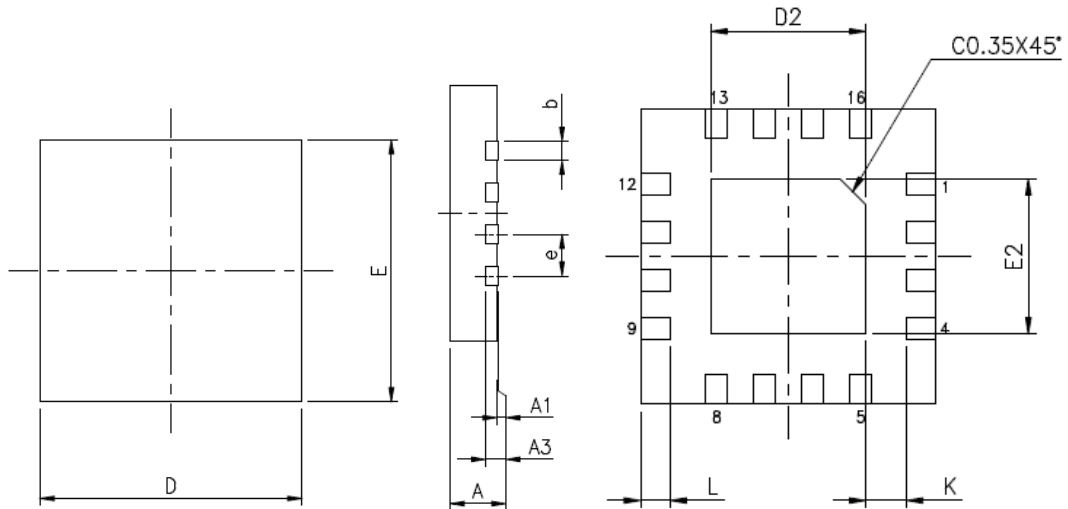


Figure 6 - QFN16 Package

Symbol	A	A1	A3	b	D	E	e	L	K	D2	E2
<b>Min</b>	0.70	0.00	0.20 REF.	0.25	4.00 BSC	4.00 BSC	0.65 BSC.	0.35	0.20	2.00	2.00
<b>Nom.</b>	0.75	0.02		0.30				0.40	-	2.10	2.10
<b>Max</b>	0.80	0.05		0.35				0.45	-	2.20	2.20

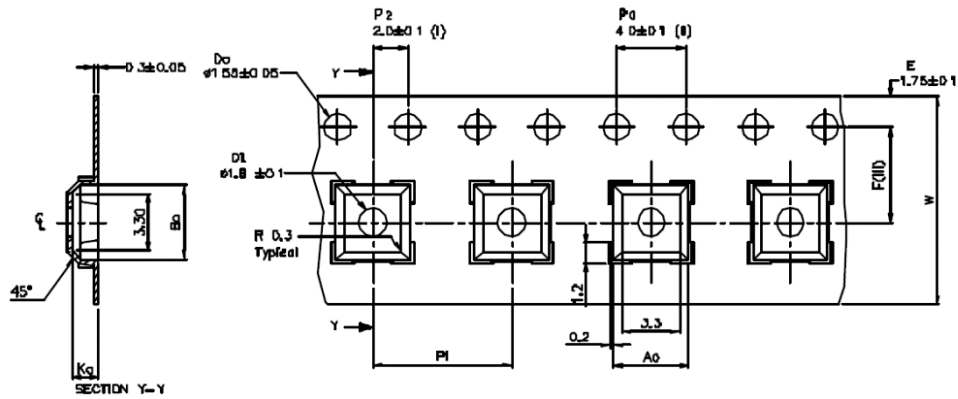
UNIT : mm

NOTES :

1. JEDEC OUTLINE : N/A.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. THE MINIMUM "K" VALUE OF 0.20mm APPLIES.
4. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

## 8 TAPE QFN16 PACKAGE

### 8.1 TAPE QFN16 PACKAGE



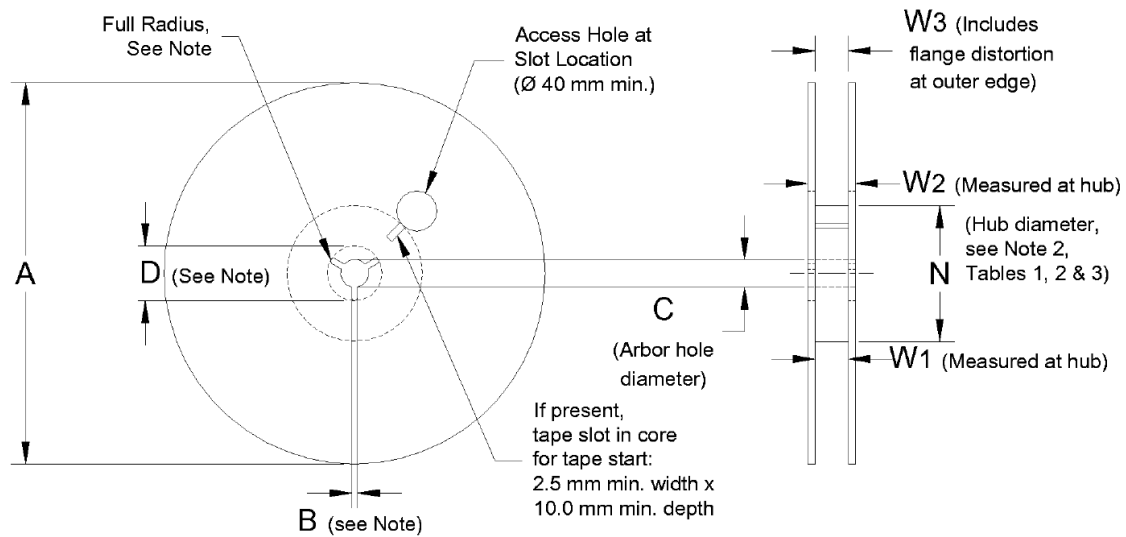
A <sub>0</sub>	4.30	+/- 0.1
B <sub>0</sub>	4.30	+/- 0.1
K <sub>0</sub>	1.50	+/- 0.1
F	5.50	+/- 0.1
P <sub>1</sub>	8.00	+/- 0.1
W	12.00	+/- 0.3

- (1) Measured from centreline of sprocket hole to centreline of pocket.
- (8) Cumulative tolerance of 10 sprocket holes is ± 0.20
- (8) Measured from centreline of sprocket hole to centreline of pocket.
- (N) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

Figure 7 – QFN16 Tape Dimensions

## 8.2 REEL INFORMATION



Note: Drive spokes optional; if used, dimensions B and D shall apply.

Figure 8 - Reel Dimension

Symbol	A	B	C	D	W <sub>1</sub> QFN24
Min	-	1.5	12.8	20.2	13.25
Typ	-	-	13.0	-	-
Max	330	-	13.5	-	13.75

## 9 ORDERING INFORMATION

Table 20 - Ordering Information

Part	Order No.	Package	Delivery	Quantity
CCG1401	CCG1401_QFN16	QFN16	Tape & Reel	5.000 per reel
CCG1401	CCG1401_CSP	CSP	On request	

## 10 REVISION HISTORY

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Revision	Date	Author	Description
1.0	31.07.2015	SL, DW	Created specification based on discussion
1.1	12.08.2015	SL	Electrical parameters revised. SPI specification added.
1.2	17.08.2015	SL	Electrical parameters revised. TRIG pin changed to COMP. Frequency adjustment for voltage amplifier added
1.3	19.08.2015	RB	Restructured SPI-section
1.4	25.08.2015	RB	Integrated SPI-changes and include of upper frequency control feature
1.5	28.08.2015	DW	Explicit description of additional standby and Vref control by digital pins Transimpedance control is now a multiplier instead divider Correct units Correct the deadtime Vsref condition Calculation formulae for lower cut-off frequency
1.6	10.09.2015	DW	3dB high-pass cut-off frequency calculation: Idc valid range added 3dB cut-off frequency values defined for max. Gain Clarification of standby modus and SPI operation
1.7	21.09.2015	RB, DW	Corrected description regarding SREF1 and SREF2 Changed Pin name from DIN to DIO and updated description Added internal signal DOUT_EN to timing diagram Add POR pin which provide an POR signal POR specification updated
1.8	27.10.2015	DW	Precise programmable comparator threshold description
1.9	03.03.2016	SL	Figure 1 has been edited
2.0	18.08.2016	KW, DW	Updated formats
	22.09.2016	DW, RB	Change default value of CTRL-register
	26.09.2016	SL	Changed max. capacitance at COMP output. Changed value of switching time from standby to operation and its symbol. Changed comparator's output slew rate and propagation time. $\Delta R_T / R_{T\_IDC}$ value is changed. Transimpedance $R_{T1, 2, 3}$ values are changed (no change in circuit is made).
2.1	13.10.2016	DW	Correct Pinning in 2.1 – 2.3 and QFN pitch 0,65mm Introduction of Start-up time (4.6) Fix condition for switch time operation – standby (4.6) Changed description of (TI) transimpedance gain default value (5.4.2) Fixed description for summing amplifier gain (GFA) = 3 (5.4.6)

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## 11 CONTENTS

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1	General Description.....	1
1.1	Features .....	1
1.2	Schematic.....	1
2	Pinout .....	2
2.1	Package QFN16 .....	2
2.2	Chip size Package .....	2
2.3	Pin Descriptions .....	3
3	Absolute Maximum Ratings.....	3
4	Electrical Characteristics.....	4
4.1	General Parameters.....	4
4.2	Power Supply .....	5
4.3	Transimpedance Input Stage / Bandwidth Limitation.....	5
4.4	Programmable Amplifier / Analog Output....	5
4.5	Comparator.....	6
4.6	Overall System Data .....	6
4.7	Power On Reset .....	7
4.8	Logic Output COMP.....	7
4.9	Logic Input (DIO, CLK, CSX).....	7
5	Functional Description .....	8
5.1	SPI and Digital Control .....	8
5.2	SPI timing .....	8
5.3	SPI Protocol.....	9
5.4	Register Description.....	9
5.4.1	Register Definitions.....	9
5.4.2	TIA (Transimpedance Register).....	9
5.4.3	GAIN (Programmable Gain Register)....	9
5.4.4	SREF1 (Programmable threshold voltage Register #1).....	10
5.4.5	SREF2 (Programmable threshold voltage Register #2).....	10
5.4.6	CTRL – General Control Register .....	10
6	Application Notes .....	11
6.1	Application with photodiode sensor.....	11
7	Package Outline.....	12
7.1	QFN16 Package .....	12
8	Tape QFN16 Package .....	13
8.1	Tape QFN16 Package.....	13
8.2	Reel Information .....	14
9	Ordering Information.....	14
10	Revision History .....	15
11	Contents .....	17