1 GENERAL DESCRIPTION

1.1 FEATURES

- IO-Link Compliant Transceiver[1]
- Integrated UART (COM1-3)
- Hardware IO-Link Stack support
- All IO-Link frame types supported
- One IO-Link slave channel with up to 200 mA driving current
- Programmable PNP-, NPN- and Push-Pull mode.
- Auxiliary multi-purpose 200mA Input-Output-Channel
- Slew rate control
- Reverse-polarity protection
- DC/DC buck converter
- Two LDO voltage regulators (programmable 3.3V/5V and 5V)
- Reference voltage output 1.2V
- Low TC on-chip oscillator with ±2% frequency accuracy
- Overcurrent protection
- Overvoltage and high temperature detection
- SPI interface
- Rich configuration options
- Evaluation board available
- QFN24 and CSP24 package

1.2 SCHEMATIC

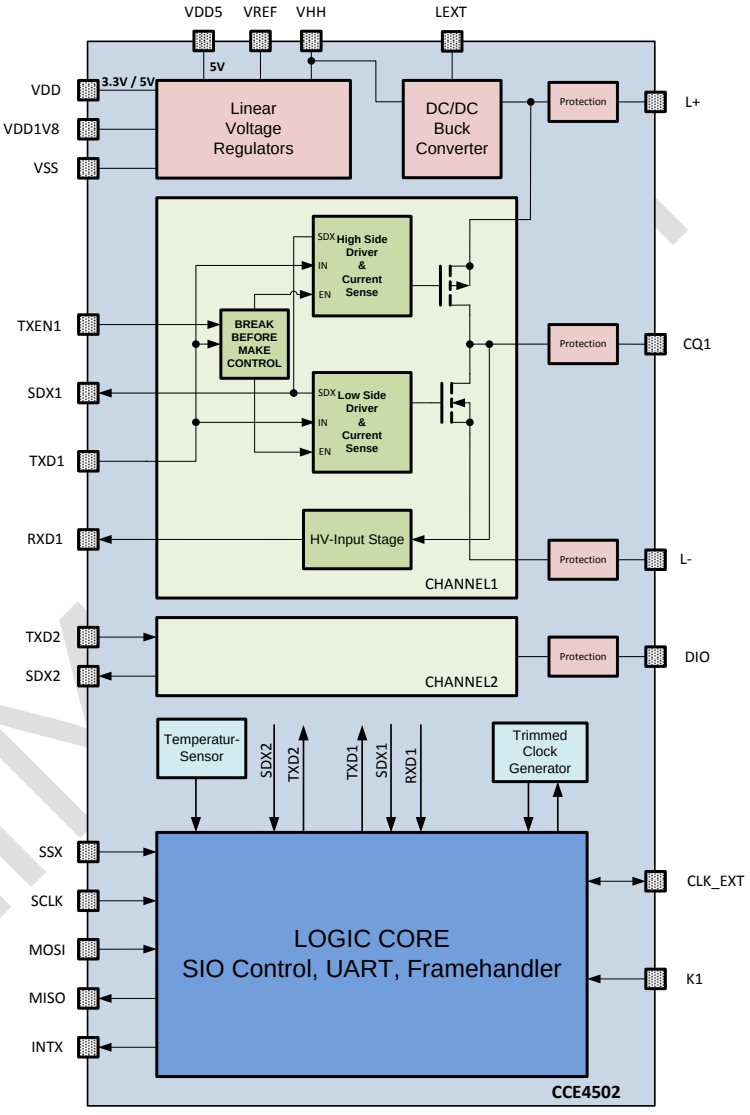


Figure 1 - Block Diagram

High-voltage interface ASSP with overvoltage, high current and high temperature protection, based on a 0.18 µm HV-CMOS technology. There are a wide range of applications that can be supported with different packaging and configuration options. Typical applications are industrial sensors and actuators.

[1] *IO-Link is a registered trademark of Profibus User Organization (PNO).*

2 PINOUT

2.1 PACKAGE

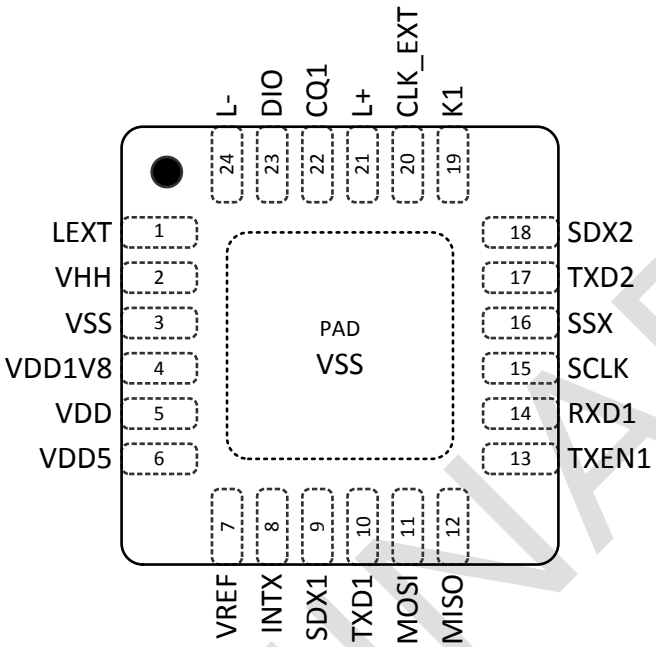


Figure 2 – QFN24 Package (4x4 mm, top view)

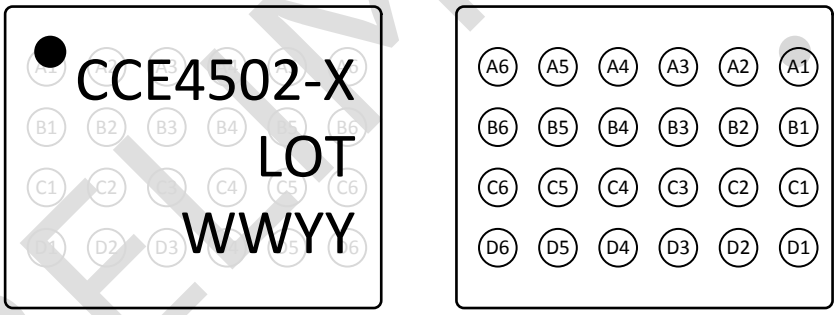


Figure 3 – Chip Scale Package (top view left, bottom view right)

2.2 PIN DESCRIPTIONS

QFN24 Pin No	CSP Pin No[2]	Name	Type	Power domain	Function	Remarks
1	D5	LEXT	PWR	VHH	DC/DC converter external inductance	
2	D4	VHH	PWR	VHH	Main supply / output DC/DC converter	
3	C4	VSS	PWR	-	Ground (Regulator)	
4	D3	VDD1V8	PWR	VDD1V8	1.8 V Supply Voltage (Internal)	
5	C3	VDD	PWR	VDD	3.3/5 V Supply Voltage Output	
6	D2	VDD5	OUT	VHH	5 V Supply Voltage Output	

[2] CSP pinout is preliminary and may change for final specification.

QFN24 Pin No	CSP Pin No[2]	Name	Type	Power domain	Function	Remarks
7	D1	VREF	OUT	VDD	Reference Voltage	
8	C1	INTX	OUT	VDD	Interrupt output	Push-pull, active-low
9	C2	SDX1	OUT	VDD	Channel 1 short detection	Push-pull, active-low
10	B1	TXD1	IN	VDD	Channel 1 signal input	Internal pull up
11	A1	MOSI	IN	VDD	SPI Master Out/Slave In	Internal hold
12	B2	MISO	OUT	VDD	SPI Master In/Slave Out	Push-pull
13	A2	TXEN1	IN	VDD	Channel 1 driver enable	Internal pull down, active-high
14	B3	RXD1	OUT	VDD	Channel 1 signal output	Push-pull
15	A3	SCLK	IN	VDD	SPI Clock	Internal pull-down
16	B4	SSX	IN	VDD	SPI Slave Select	Internal pull-up
17	A4	TXD2	IN	VDD	Channel 2 signal input	Internal pull-up
18	A5	SDX2	OUT	VDD	Channel 2 short detection	Push-pull, low active
19	B5	K1	IN	VDD	Configuration bit 1	Internal pull down
20	A6	CLK_EXT	IN/OUT	VDD	External clock input / Clock output	Push-pull
21	B6	L+	PWR	L+	Positive supply (IO-Link)	
22	C6	CQ1	IN/OUT	L+	IO-Link data channel 1	
23	D6	DIO	IN/OUT	L+	Switching Input / Output channel 2	
24	C5	L-	PWR	L+	Ground supply (IO-Link)	
PAD	-	VSS	PWR	-	Ground	Internally connected to QFN24 pin 3

Table 1 - Pin Descriptions

3 ABSOLUTE MAXIMUM RATINGS

T_{amb} = 25°C+/-1°C unless otherwise specified.

Parameter	Conditions	Name	Min	Typ	Max	Unit
Supply Voltage	Static, referenced to V_{L-}	V_{L+} -V_{L-}	-40		40	V
Supply Voltage	dynamic (t <= 100ms)	V_{L+} -V_{L-_pulse}	-50		50	V
VHH pad max voltage	Referenced to VSS	$V_{VHH,max}$	-0.3		(V_{L+} -V_{L+}) +0.3V	V
Power Dissipation	QFN24 Package on Multilayer PCB	P_{TOT}			1	W
Operating Temperature	Ambient temperature	T_{amb}	-40		105	°C
Storage Temperature		$T_{storage}$	-55		155	°C
Junction Temperature		T_j	-50		150	°C
Voltage at pin CQ1/DIO	Referenced to V_{L-}: V_{CQ}-V_{L-}	$V_{CQ,max}$	-0.3		(V_{L+} -V_{L-}) +0.3	V
Voltage at all other pins	Referenced to VSS	$V_{...max}$	-0.3		V_{DD}+0.3	V
ESD protection	JS-001-2012 HBM	V_{ESD}	4			kV
	JEDEC JESD78D Class1	$I_{latchup}$	100			mA
Soldering Temperature	12 s max.	T_{solder}			260	°C
FIT Rate	$T_{amb,max}$=70°C				50	FIT

Table 2 - Absolute Maximum Ratings

4 ELECTRICAL CHARACTERISTICS

T_{amb} = -40°C ... 105°C, V_{L+}-V_{L-} = 24 V unless otherwise specified.

4.1 GENERAL PARAMETERS

Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
Over temperature flag	$t_{deglitch}$=4096/fclk		T_{flag}	110	120	130	°C
Over temperature flag hysteresis			T_{hyst}	11		19	°C
Over voltage flag threshold	V_{L+} rising	21, 24	$V_{L+,thr+}$	38	40	42	V
Main Supply Voltage	DC/DC enabled (Supply Mode 1)	21, 24	V_{L+} -V_{L-}	9		36	V
LDO Input Voltage	DC/DC disabled (Supply Mode 2 or Supply Mode 3)	2,3	V_{VHH} -V_{VSS}	6		36	V
Supply voltage ripple	F_{ripple} = DC ... 100kHz	21	ΔV_{L+}			1.3	V_{p-p}
Quiescent Main Current	V_{L+} -V_{L-} = 24V	21, 24	I_{L+}			5	mA
Quiescent LDO Current	V_{VHH} -V_{VSS} = 7V	2, 3	I_{VHH}			2	mA
External capacitor VHH	DC/DC enabled, max. ESR=100m Ω	2, 3	$C_{VHH,DCDC}$	10			µF
	DC/DC disabled (Supply Mode 2)	2, 3	C_{VHH}	1			nF
External capacitor VDD		5, 3	C_{VDD}	220	470		nF
External capacitor VDD5		6, 3	C_{VDD5}	47	100		nF
External capacitor VDD1V8	Between VDD1V8 and VSS	4, 3	C_{VDD1V8}	47	100		nF
Inductance DC/DC Converter		1, 2	L_{EXT}		22		µH
System clock frequency		20	F_{clk}	-2%	14.745	+2%	MHz
Reference Voltage	T_{amb}=25°C, $I_{load,REF}$ < 100uA	7, 3	V_{REF}	1.15	1.2	1.35	V
Reference Voltage Temperature Coefficient		7, 3	TK_{VREF}			40	ppm/K

Table 3 - General Parameters

4.2 3.3V/5V VOLTAGE REGULATOR

Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
Output Voltage VDD	5 V (CCE4502 – 5V)	5, 3	VDD_{5V}	4.75	5	5.25	V
	3.3 V (CCE4502 – 3.3V)	5, 3	VDD_{3V3}	3.1	3.3	3.5	V
Temperature Coefficient VDD		5, 3	TK_{VDD5}			150	ppm/K
Voltage Drop	Load Current = 25mA	2, 5	V_{VHH}-V_{VDD}	0.7			V
Output Current VDD		5	I_{VDD}			50	mA
Line regulation VDD	I_{VDD} = 10mA, 9V< VL+<36V (Supply mode 1 and 2)	5, 3				10	mV
	I_{VDD} = 10mA, 6V< VHH<36V (Supply mode 3)					100	
Load regulation VDD	DC current up to 50mA	5, 3				0.4	%
Power Supply Rejection Ratio	V_{L+}/V_{VDD}, C_{VHH}=10µF, C_{VDD}=220nF, ESR=1 Ω, f<200kHz	5, 3	PSRR	50			dB
	V_{VHH}/V_{VDD}, C_{VDD}=220n, ESR=1 Ω, f<200kHz			40			
Power-On Threshold	Referenced to VDD target voltage (3.3V or 5V)	5, 3	V_{RST}	85	90	95	%
Start-up time	After V_{L+} exceeds minimum value	5, 3	$t_{start-up}$			1	ms
	Glitch blanking		t_{glf}		1		us

Table 4 - Linear Regulator 3.3V/5V

4.3 5V VOLTAGE REGULATOR

Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
Output Voltage VDD5		6, 3	VDD5	4.75	5	5.25	V
Temperature Coefficient		6, 3	TK_{VDD5}			150	ppm/K
Voltage Drop	Load Current = 5mA	2, 6	V_{VHH}-V_{VDD5}	0.7			V
Output Current VDD5		6	I_{VDD}			10	mA
Line regulation VDD5	I_{VDD5} = 5mA, 7.5V< VL+<36V	6, 3				10	mV
Load regulation VDD5	DC current up to 5mA	6, 3				0.2	%
Power Supply Rejection Ratio	V_{L+}/V_{VDD5}, C_{VDD5}=100nF, f<200kHz		PSRR	40			dB

Table 5 - Linear Regulator 5V

4.4 DC/DC CONVERTER

Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
Output Voltage VHH	DC/DC in buck mode	2, 3	VHH_{DCDC}	5.5	7	8.5	V
Output Voltage LEXT	DC/DC in linear mode, VHH and LEXT shorted	1, 3	$V_{LEXT,LDO}$	5.5	7	8.5	V
Ripple VHH	L_{EXT}=22µH, C_{VHH} = 22µF, ESR_{CVHH} = 50mΩ, I_{VHH}=60mA	2	$V_{VHH,pp}$			50	mV
Switching Frequency DC/DC Converter	DC/DC in buck mode		f_{SWITCH}	1.5		2.5	MHz
DC/DC Output Current		2	$I_{DCDC,out}$			60[3]	mA
Line regulation VHH	I_{VHH} = 1mA, 9V< V_{L+} <24V	2				10	%
Load regulation VHH	DC current up to 60mA	2, 3				1	%

Table 6 - DC/DC Converter

4.5 INPUTS / OUTPUTS CQ1, DIO

Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
Voltage CQ1/DIO		22, 23	V_{CQ_MAX}			36	V
Output voltage low level	active pull down, I_{OL}=-200mA	22, 23	V_{OL}			2	V
Output voltage high level	active pull up, I_{OH}=+200mA	22, 23	V_{OH}	V_S-2			V
Leakage current	input enabled	22, 23	I_{leak}	-100		100	µA
Maximum Permanent Output Current	Current per CQ channel	22, 23	I_{CQmax}			200[3]	mA
Output source current limit	SLEW=0 (see section 5.8.5)	22, 23	I_{limP}			340	mA
Output sink current limit		22, 23	I_{limN}			320	mA
Overcurrent detection threshold	Source/sink current, SLEW=0	22, 23	I_{OC}		210		mA
Peak short circuit current	V_{L+} -V_{L-}=36V Up to 1µs after short	22, 23	$I_{short,peak}$			2	A
Load capacitance	COM1 or COM2	22, 23	C_L			5	nF
Inductive load		22, 23	L_{Load}			50	mH
Output slew rate rise/fall	Open load, SLEW=0	22, 23	$r_{slew,open}$	42	60	100	V/µs
	5nF Load, SLEW=0	22, 23	$r_{slew,5nF}$	20		40	V/µs
Switch On Time		22, 23	$t_{DLY\_LH,1nF}$			500	ns
Switch Off Time		22, 23	$t_{DLY\_HL,1nF}$			500	ns
Break before Make Delay		22, 23	t_{LH_BBM}, t_{HL_BBM}	1		30	ns
Short Circuit Detection Time	see H/V configuration register	22, 23	$t_{OVLDDET}$	100			µs
Input threshold high level	CQ1/DIO	22, 23	V_{IH}	10.5		13	V
Input threshold low level		22, 23	V_{IL}	8		11.5	V
Hysteresis between input thesholds high and low		22, 23	V_{Hyst}	1			V

Table 7 - Switching Outputs

[3] Consider devices total power consumption (see 6.1).

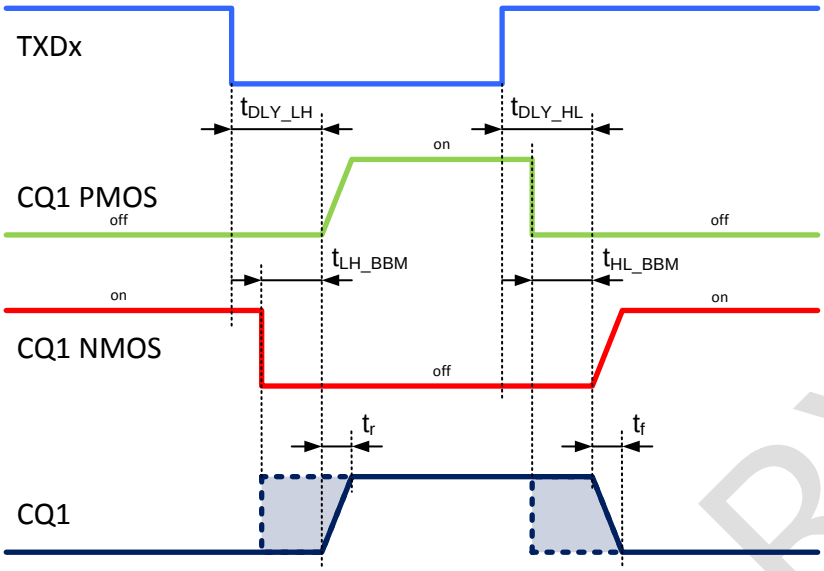


Figure 4 - Timing CQ1 Outputs ("Break before Make")

The solid line of CQ1 signal in Figure 4 describes the typical or best case scenario. Depending on the external circuitry, the slew rate can differ from this. This is shown by the shaded area e.g. an external pull-up pulls CQ1 high as soon as the NMOS is switched off.

4.6 IO LINK PROTOCOL

Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
Transmission rate	COM1 COM2 COM3		f_{DTR}		4,8 38,4 230,4		kbit/s
Bit time	COM1 COM2 COM3		T_{BIT}		208,3 26,0 4,34		µs
UART frame transmission delay of the Device			T_{dD}	0		3	T_{BIT}
Response time of Devices			T_{Dev_resp}	1		10	T_{BIT}
Cycle time	M-sequence Type_2_1 COM1 COM2 COM3		T_{CYC}	 18 2,3 0,4			ms

Table 8 - IO Link specification

4.7 DIGITAL I/O

Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
Input Voltage LOW	V_{DD} - V_{SS} = 3.3 V	11, 13, 15, 16, 17, 19, 20	$V_{IN\_L\_3V3}$			1.5	V
Input Voltage HIGH	V_{DD} - V_{SS} = 3.3 V	11, 13, 15, 16, 17, 19, 20	$V_{IN\_H\_3V3}$	1.8			V
Input Voltage LOW	V_{DD} - V_{SS} = 5.0 V	11, 13, 15, 16, 17, 19, 20	$V_{IN\_L\_5V}$			2.1	V
Input Voltage HIGH	V_{DD} - V_{SS} = 5.0 V	11, 13, 15, 16, 17, 19, 20	$V_{IN\_H\_5V}$	2.9			V
Input Capacitance		11, 13, 15, 16, 17, 19, 20	C_{IN}			5	pF
Input Leakage Current		11, 13, 15, 16, 17, 19, 20	I_{ILEAK}	-5		5	µA
Input Pull-Up current	V_{DD} - V_{SS} = 3.3 V, V_{pin}=0V	11, 16, 17	I_{PU_3V3}	10		40	µA
Input Pull-Up current	V_{DD} - V_{SS} = 5.0 V, V_{pin}=0V	11, 16, 17	I_{PU_5V}	25		100	µA
Input Pull-Down current	V_{DD} - V_{SS} = 3.3 V, V_{pin}=3.3V	13, 15, 19, 20	I_{PD_3V3}	20		70	µA

Input Pull-Down current	V_{DD} - V_{SS} = 5.0 V, V_{pin}=5.0V	13, 15, 19, 20	I_{PD_5V}	20		70	µA

Table 9 - Digital Inputs

Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
Output Voltage LOW	V_{DD} - V_{SS} = 3.3 V I_{OUT_LOW} = 2 mA	8, 9, 12, 18, 20	V_{OUT_L}			0.5	V
	V_{DD} - V_{SS} = 5.0 V I_{OUT_LOW} = 2 mA	8, 9, 12, 18, 20	V_{OUT_L}			0.5	V
Output Voltage HIGH	V_{DD} - V_{SS} = 3.3 V I_{OUT_HIGH} = 2 mA	8, 9, 12, 18, 20	V_{OUT_H}	2.8			V
	V_{DD} - V_{SS} = 5.0 V I_{OUT_HIGH} = 2 mA	8, 9, 12, 18, 20	V_{OUT_H}	4.5			V
Output Leakage Current	Tristate active	8, 9, 12, 18, 20	I_{OLEAK}	-5		5	µA
Output Capacitance		8, 9, 12, 18, 20	C_{OUT}		5		pF

Table 10 - Digital Outputs

5 FUNCTIONAL DESCRIPTION

5.1 OVERALL FUNCTIONAL DESCRIPTION

The IC integrates one IO-Link capable bidirectional switching interface connected to CQ1. It can be used as a SIO, UART transceiver or IO-Link slave port. It includes a hardware IO-Link frame handler based on the UART interface which provides IO-Link protocol handling facilities. The pin DIO is configured as an output. Both pins, CQ1 and DIO, can be individually configured as push-pull or open drain (PMOS or NMOS).

The CCE4502 is controlled via IO-Pins or the SPI.

The logic core is clocked by an integrated oscillator. An external clock can be provided at pin CLK_EXT. Therefore, a frequency of 14.745 MHz is required.

5.2 PROTECTION CIRCUITRY

The CCE4502 has following protection circuitry:

1. The CQ1 and DIO outputs, the L+ and L- Pins are protected against ESD.
2. The CQ1 and DIO outputs, the L+ and L- Pins are protected against reverse polarity connection.
3. Both paths to L+ and L- are protected against overcurrent.
4. On-chip over temperature is detected and notified.

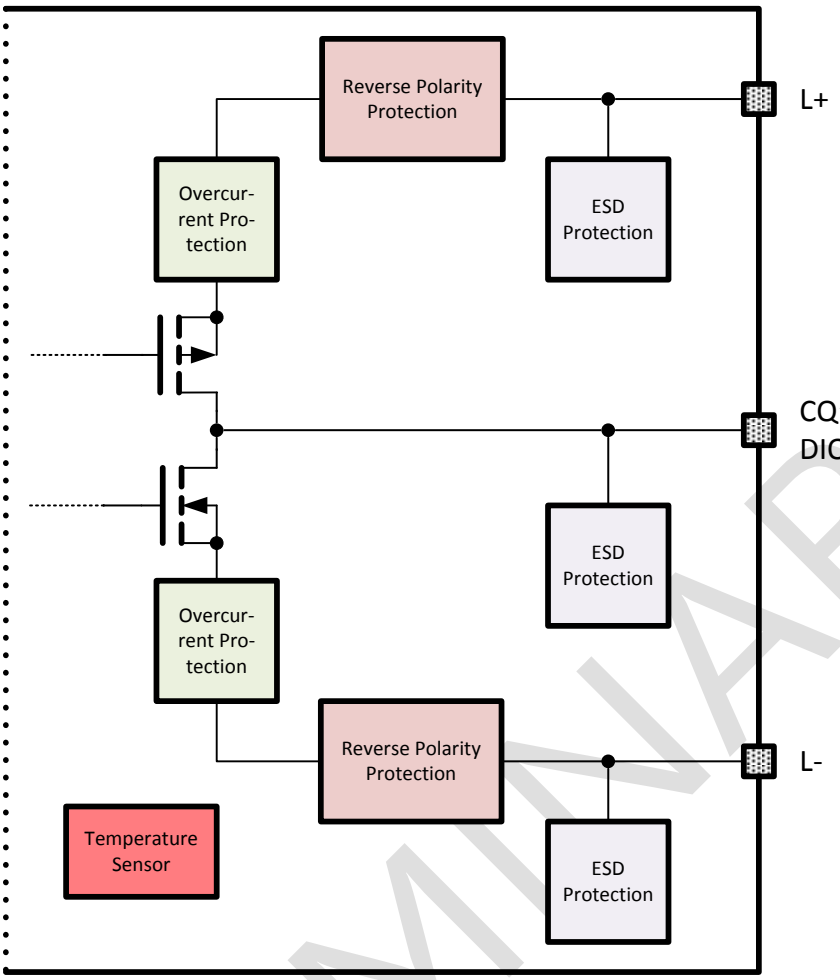


Figure 5 - Protection circuitry at CQ1, DIO, L+ and L-

5.3 POWER SUPPLY

Five regulators are implemented for the power supply of the IC and external components.

1. A DC/DC converter at pin LEXT/VHH which is permanently configured for Buck or Linear mode. This converter may supply external circuitry.
2. A LDO at pin VDD, which is permanently configured for 3.3V or 5V output voltage, and can supply external circuitry.
3. A 5V-LDO (VDD5). This regulator may supply external circuitry.
4. A core supply regulator (1.8V) at pin VDD1V8. External load must not be connected to the regulator output.
5. A buffered bandgap reference voltage is provided at pin VREF.

NOTE: Always calculate the maximum IC junction temperature to decide if the IC can supply the required currents for external circuitry. In particular, the IO-Link output stage currents, LDOs supply currents and thermal coupling of the IC to the PCB will impact the junction temperature.

5.3.1 DC/DC converter, Supply Modes

A DC/DC converter is provided which either acts as a buck mode switching converter, requiring an external inductor, or as a linear regulator. The function of the converter is factory preprogrammed (see Ordering Information).

The main purpose of the buck converter mode is to limit the on chip power dissipation by converting the main supply voltage at L+ and L- to an intermediate level of about 7V (Supply Mode 1, see Figure 13). The buck converter is designed for an external 22µH inductor between pins LEXT and VHH. A 22µF capacitor is required between pins VHH and VSS to buffer the buck converters output. A 10µF capacitor is recommended between L+ and VSS, see Figure 6. The inductors saturation current must be above the buck converters output current limit of 60mA. The buck converters output can be used to drive external circuitry connected to pin VHH. In total a maximum external load current of 50mA can be drawn from VHH and VDD.

If the DC/DC converter is configured for linear regulation mode it provides about 7V at LEXT. LEXT and VHH must then be connected externally (Supply Mode 2, see Figure 14). A 1µF output capacitor is required at pins LEXT and VSS.

If the DC/DC converter is not required by the application, leave pin LEXT floating. The 3.3V/5V and 1.8V regulators must then be supplied by an external supply connected to pin VHH (Supply Mode 3, see Figure 15).

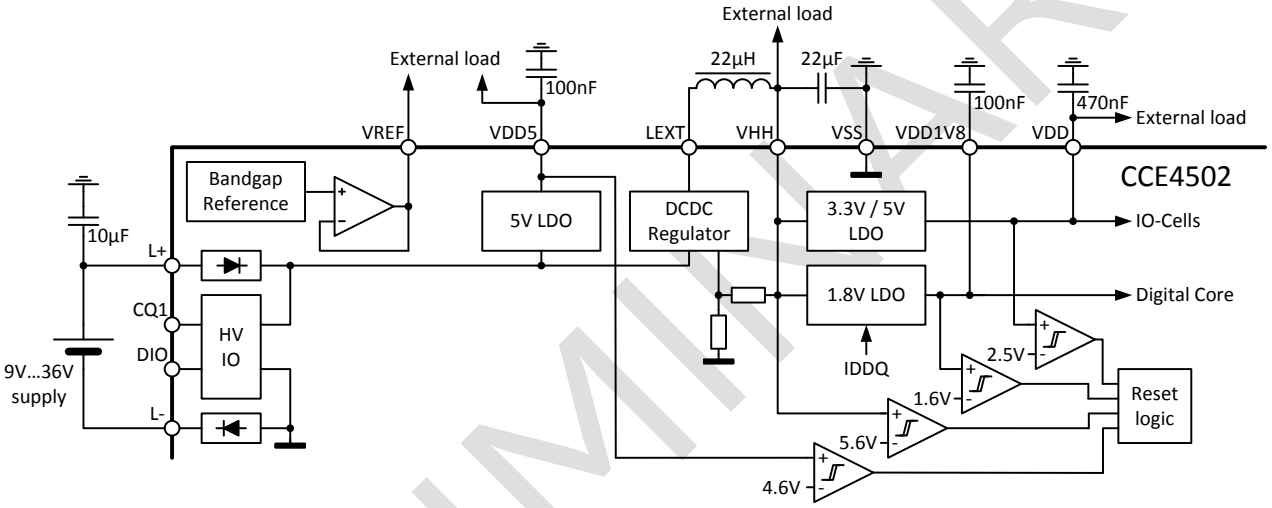


Figure 6 – Power supply block diagram (Supply Mode 1)

5.3.2 3.3V/5V LDO

The 3.3V/5V LDO provides power for all logic level in- and outputs (pins 8 to 20) at pin VDD. The output voltage (3.3V or 5V) is permanently programmed during the final test of the IC. See section 9 for corresponding order codes.

A 220nF capacitor from pin VDD to VSS is required to provide transient currents for switching outputs.

The LDO input is connected to VHH, which can be supplied by the on chip DC/DC converter or an external supply. See Figure 13, Figure 14 and Figure 15 for possible connection options.

The LDO output can supply external circuitry (e.g. microcontrollers). In total a maximum external load current of 50mA can be drawn from VHH and VDD. Always verify that the ICs maximum junction temperature is exceeded, when using the regulator outputs for external load.

5.3.3 1.8V Linear Regulator

The 1.8V regulator provides power for internal logic blocks. A 100nF capacitor from pin VDD1V8 to VSS is required. Do not connect external load to pin VDD1V8.

5.3.4 5V LDO

A 5V LDO provides power for internal and external circuitry at pin VDD5. The LDO input is connected to pin L+ through the reverse polarity protection. A 100nF capacitor from pin VDD5 to VSS is recommended. External load connected to VDD5 must not draw more than 10mA.

5.3.5 Bandgap Reference Output

An internal bandgap circuit provides internal and external trimmed reference voltage at pin VREF. External load at pin VREF must not draw more than 100µA.

5.4 POWER-ON RESET

The power on reset circuitry supervises the main (L+/L-), IO (3.3V/5V) and core (1.8V) supplies to ensure proper initialization of all registers (see Figure 6). If the internal power on reset signal is activated, the logic core is reset to defaults and all outputs are in high impedance state.

A glitch filter is implemented to suppress supply voltage sags shorter than t_{glf}. See Figure 7.

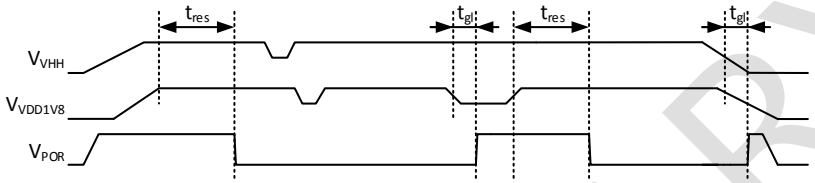


Figure 7 – Power-On Reset timing (only core voltage 1.8V POR depicted)

5.5 CONFIGURATION PIN K1

A configuration pin K1 defines whether the internal or an external oscillator is used to clock the control logic. If an external clock is used the internal clock generator is disabled.

Pin K1 has an internal pull down to use the internal clock if K1 is not connected externally. Table 11 lists configuration options. It is recommended to connect pin K1 to VSS or VDD externally for best reliability.

K1	CLK_EXT	Functional Mode
VSS	Output	Functional Mode using internal oscillator (default)
VDD	Input	Functional Mode using external crystal oscillator

Table 11 – K1 Configuration Bit

5.6 HV-IO STAGES

Two identical output stages drive the channel 1 and channel 2 pins (CQ1/DIO). Each output transistor pair has individual slew rate control and current limiting circuitry. The output slew rate, output current limit and output overcurrent detection threshold can be adjusted for each channel via the SLEW1/2 registers (5.8.5). The control logic is shown in Figure 8.

Channel 1 provides an input buffer compatible to the IO-Link standard. The input buffer can be disabled via the CONF1.DIS register. See Table 12.

CQ1	CONF1.DIS	RXD1
High	0	0
Low	0	1
X	1	1

Table 12 - Channel 1 input buffer truth table

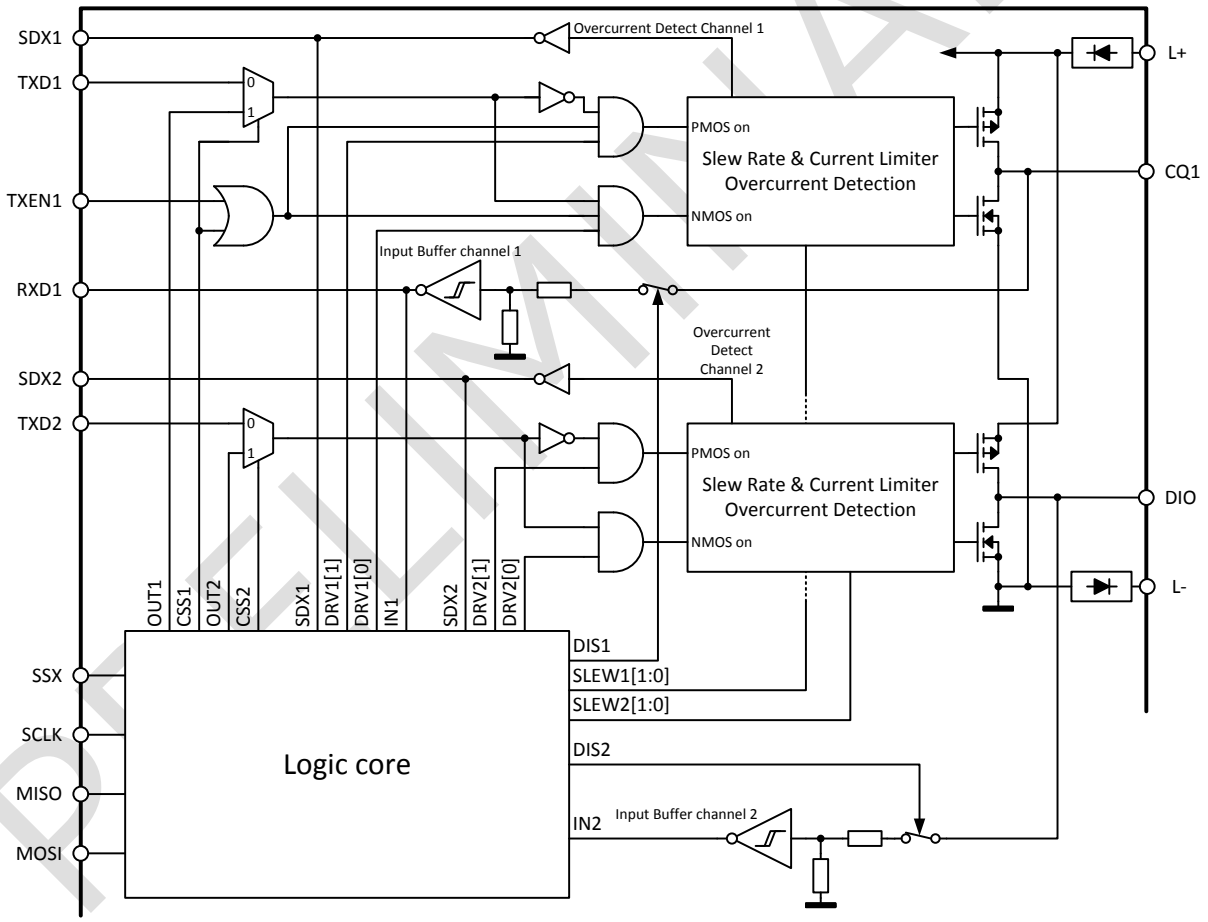


Figure 8 – HV-Output stage

If the output current of channel 1 or channel 2 exceeds the output current limit defined via the SLEW1/2 registers (5.8.5), an overcurrent detection signal is available at SDX1 and SDX2 respectively. The logic core also receives this information and disables the output stages if configured in OVLD1/2 registers (see 5.8.4).

Output state	SDXx
Output current below overcurrent detection threshold	1
Output current above overcurrent detection threshold	0

Table 13 Overcurrent detection truth table

Each channel can be controlled either by dedicated control pins (TXD1, TXEN1, TXD2) or the SPI interface. The registers CONF1.CSS (5.8.2) CONF2.CSS (5.8.3) define if the outputs are controlled by the dedicated pins or SPI. This allows the IC to be used as level shifter only, without using the SPI interface.

The logic core defines the configuration of the output stages (High-Z, Open-Drain, Push-Pull) via the CONF1.DRV (5.8.2) and CONF2.DRV (5.8.3) registers. Default values of these registers are programmed during final test of the IC. A One-Time-Programmable memory element (fuse) is used to store this information. The memory content cannot be changed after the ICs final test. Changing the CONF1 and CONF2 registers in the application requires SPI access.

To control the output stages via SPI only, the registers CSS1 and CSS2 must be set to one, thus ignoring the dedicated control pins (TXD1, TXEN1, TXD2). See Table 14 and Table 15 for the full output stages logic.

TXEN1	TXD1	CONF1.CSS	SIO1.OUT	CONF1.DRV[1:0]	CQ1
1	0	0	X	0	High-Z
1	0	0	X	1	High-Z
1	0	0	X	2	High
1	0	0	X	3	High
1	1	0	X	0	High-Z
1	1	0	X	1	Low
1	1	0	X	2	High-Z
1	1	0	X	3	Low
0	X	0	X	X	High-Z
X	X	1	0	0	High-Z
X	X	1	0	1	High-Z
X	X	1	0	2	High
X	X	1	0	3	High
X	X	1	1	0	High-Z
X	X	1	1	1	Low
X	X	1	1	2	High-Z
X	X	1	1	3	Low

Table 14 Channel 1 output stage truth table

TXD2	CONF2.CSS	SIO2.OUT	CONF2.DRV[1:0]	DIO
0	0	X	0	High-Z
0	0	X	1	High-Z
0	0	X	2	High
0	0	X	3	High
1	0	X	0	High-Z
1	0	X	1	Low
1	0	X	2	High-Z
1	0	X	3	Low
X	1	0	0	High-Z
X	1	0	1	High-Z
X	1	0	2	High
X	1	0	3	High
X	1	1	0	High-Z
X	1	1	1	Low

X	1	1	2	High-Z
X	1	1	3	Low

Table 15 Channel 2 output stage truth table

5.7 OPERATIONAL MODES

There are three possible operational modes for channel1 – Standard I/O, UART and Frame Handler (IO-Link[4]) Mode. The channel mode can be configured via the MODE-bits of the CONF1 register (see 5.8.2). Channel 2 is always in Standard I/O mode. The desired output stage, N, P or Push-Pull driving, can be configured via the DRV-bits of the CONF1/2 register.

5.7.1 Standard I/O (SIO)

If a channel is configured in the Standard I/O Mode, the output driver can be directly controlled via the OUT-bit of register SIO1/2 (5.8.6 and 5.8.7). The IO-bit of SIO1 reflects the current state of the CQ1 pin.

In this mode, it is also possible to control and observe the channel using the TXD1/2, TXEN1 and RXD1 pins. To distinguish between pin- and logic-control, the Channel-Source-Select-bit (CSS) of register CONF1/2 has to be set accordingly.

Since the sense of TXD1/2 to CQ is inverted, it is possible to connect a standard microcontroller UART interface with a high idle state to the TXD/RXD pins.

5.7.2 UART

The UART mode of channel 1 is designed to send and receive 8 bits of data per character followed by an even parity bit. If this mode is enabled the used COM speed needs to be set in the CONF1 register.

By default, the channel will listen for incoming UART transactions at the CQ1 pin. If a character is received, an interrupt is triggered and the data can be read back from the UART register (5.8.8). A transaction is started by writing the data to the UART register.

The received UART data is not buffered. Receiving multiple characters, while not reading them back, causes data loss. This will be indicated by the OFLW-bit in the STAT-register (5.8.18).

5.7.3 Frame Handler (IO-Link Mode)

The Frame Handler Mode extends the UART interface. It is required to define the used COM speed in the CONF1 register.

It mostly automates the transaction of frames, defined by the IO-Link protocol. Therefore an automated CRC check for incoming, and an automated CRC computation for outgoing messages is integrated. The frame handler will also monitor the specified timing constraints and takes care to comply with them as well.

5.7.3.1 Configuration

The device message lengths of each frame is influenced by the ODL, MPDL and DPDL registers, but is also depending on the access type, addressed channel and frame type which are defined in the second byte of each IO-Link frame. FT0 frames always use one byte on-request data. FT1 frames use the MPDL or DPDL lengths, if the address channel is the Process Data Channel; otherwise the ODL length is used. FT2 frames always use the MPDL, DPDL and ODL lengths (see Figure 9).

[4] „IO-Link Interface and System" Specification Version 1.1.2, July 2013

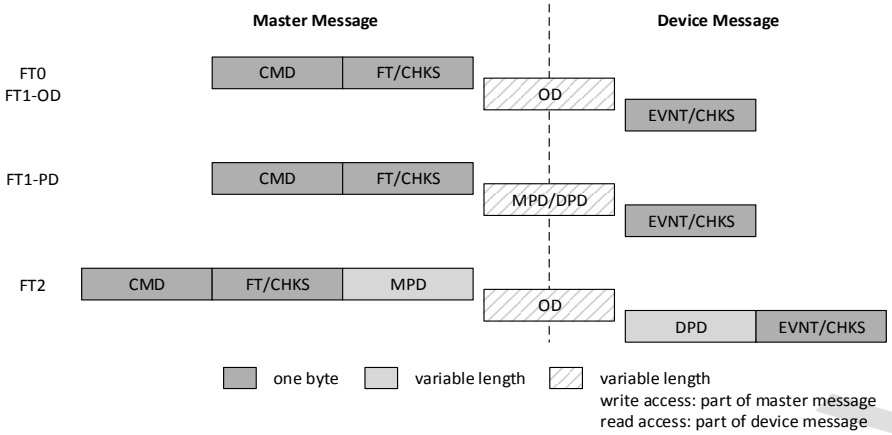


Figure 9 - Frame Lengths

The frame handler listens for incoming master transactions and triggers an interrupt if a part or the complete device message is received. The interrupt behavior can be modified using the INT_EN_FH (5.8.26) and TRSH (5.8.15) register. The received data can be read back via the FHD register (5.8.14) by multiple SPI transactions or single/multiple bulk SPI transactions.

After successfully receiving an incoming master message, the frame handler waits for the user to write the complete message data into the frame buffer via the FHD register. This can be done by multiple SPI transactions or by a single bulk SPI transaction. The transaction always starts immediately after the first byte is written into the frame buffer.

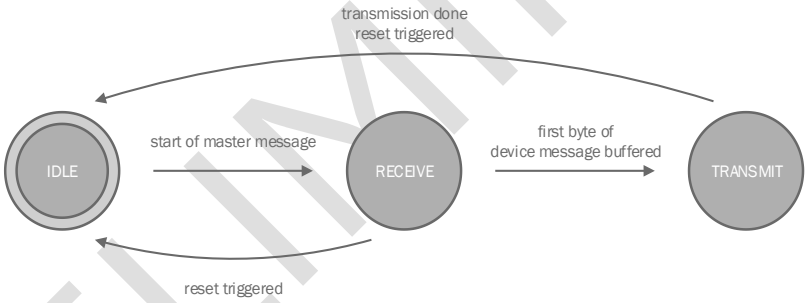


Figure 10 - Transaction Sequence

5.7.3.2 Skip and Reset Function

It is possible to reset the frame handler or skip an invalid frame from any state. This can be done by writing '1' to the RST- or SKIP-bit of the FHC register (5.8.9). Skipping a frame causes the frame handler to ignore the rest of an incoming message, without triggering any additional interrupt. A soft reset is done after receiving the rest of the invalid message or if a timeout was detected. Resetting a frame will immediately reset the frame handler into its idle state.

5.8 REGISTER DESCRIPTION

5.8.1 Register Definitions

Address	Name	Description
0x00-0x1F	-	reserved
Channel 1 Regs		
0x20	CONF1	Channel Configuration
0x21	OVLD1	Overload Protection
0x22	SLEW1	Slew Rate Control
0x23	SIO1	SIO Control
0x24	UART	UART Data
0x25	FHC	Frame Handler Control
0x26	ODL	On-Request Data Length
0x27	MPDL	Master Process Data Length
0x28	DPDL	Device Process Data Length
0x29	BLVL	Frame Handler Buffer Level
0x2A	FHD	Frame Handler Data
0x2B	-	reserved (must not be used by future regs)
0x2C-0x2D	-	reserved
0x2E	TRSH	Threshold Level Interrupt Triggering
0x30-0x3F	-	reserved
Channel 2 Regs		
0x40	CONF2	Channel Configuration
0x41	OVLD2	Overload Protection
0x42	SLEW2	Slew Rate Control
0x43	SIO2	SIO Control
0x44 – 0x5FE	-	reserved
Common Regs		
0x60	REV	Revision Code
0x61	PROT	Channel Protection
0x62	STAT	Channel Status
0x63	INT_SRC_STAT	Status Interrupt sources
0x64	INT_EN_STAT	Status Interrupt enables
0x65	INT_SRC_SIO	Interrupt sources of SIO-mode
0x66	INT_EN_SIO	Interrupt enables of SIO-mode
0x67	INT_SRC_UART	Interrupt sources of UART-mode
0x68	INT_EN_UART	Interrupt enables of UART-mode
0x69	INT_SRC_FH	Interrupt sources of FH-mode
0x6A	INT_EN_FH	Interrupt enables of FH-mode
0x6B	-	reserved
0x6C	CLK_OUT	Output-Clock control
0x6D – 0x7F	-	reserved

Table 16 - Register Definitions

5.8.2 CONF1 (0x20)

This is the configuration register for the IO-Link-channel (channel1). It is possible to configure the channel mode and the communication speed used by the integrated UART, or to generally disable the input stage. Further the channel source and the output stage type can be configured. The output stage can be configured as P-, N-Mode or Push-Pull.

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DIS	DRV		CSS	COM		MODE	
Access	R/W	R/W		R/W	R/W		R/W	
Default	0	00b		0	0		0	

Table 17 – CONF1 register

MODE *Channel Mode*

0h: SIO Mode (default)

1h: UART Mode
2h: Frame Handler (IO-Link) Mode
3h: reserved

COM *UART communication mode*

0h: UART disabled (default)
1h: COM1 (4.8 kBit/s)
2h: COM2 (38.4 kBit/s)
3h: COM3 (230.4 kBit/s)

CSS *Channel Source Select*

0: Channel inputs TXD1 and TXEN_1 are controlled via pins
1: Channel inputs TXD1 and TXEN_1 are controlled via internal logic core

DRV *Output stage configuration*

00b CQ1 disabled
01b N-Mode
10b P-Mode
11b Push-Pull

DIS *IO-Link input stage disable*

0: Input stage enabled
1: Input stage disabled (RXD1 = 1)

5.8.3 CONF2 (0x40)

This is the configuration register for channel2. The channel source and the output stage type can be configured. The output stage can be configured as P-, N-Mode or Push-Pull.

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	DIS	DRV		CSS	reserved			
Access	R/W	R/W		R/W	-			
Default	0	00b		0	-			

Table 18 - CONF2 - register

CSS *Channel Source Select*

0: Channel input TXD2 is controlled via pins
1: Channel input TXD2 is controlled via internal logic core

DRV *Output stage configuration*

00b DIO disabled
01b N-Mode
10b P-Mode
11b Push-Pull

DIS *IO-Link input stage disable*

0: Input stage enabled
1: Input stage disabled

5.8.4 OVLD1/2 (0x21/0x41)

This is the configuration register for the detection of a high channel load. The detection time of high load and the corresponding disable time of a channel can be configured. If the automatic channel disable

function is active and an overcurrent condition at this channel is present for t_{OVLDET}, the channel gets disabled. After $t_{OVLDDIS}$ passed, the channel is enabled again.

CAUTION: Disabling this feature may cause damage to the device!

$$t_{OVLDDET} = 100us * (1 + MULT)$$

$$t_{OVLDDIS} = 100us * (1 + MULT) * FACTOR$$

Bit	7	6	5	4	3	2	1	0
Name	ADIS		MULT					
Access	R/W		R/W					
Default	11b		000000b					

Table 19 - OVLD register

ADIS *Automatic Channel Disable*

0h: disabled
1h: enabled, FACTOR is 10
2h: enabled, FACTOR is 100
3h: enabled, FACTOR is 1000

MULT *Multiplier Value*

5.8.5 SLEW1/2 (0x22/0x42)

This is the slew rate control register for the IO-Link device.

Bit	7	6	5	4	3	2	1	0
Name	Reserved						SLEW	
Access	-						R/W	
Default	-						0	

Table 20 - SLEW register

SLEW *CQ Output slew rate, current limit and overcurrent detection threshold control*

0h: Slew rate: 60V/µs	Current limit: 300mA	Overcurrent threshold: 210mA (default)
1h: Slew rate: 30V/µs	Current limit: 150mA	Overcurrent threshold: 105mA
2h: Slew rate: 20V/µs	Current limit: 100mA	Overcurrent threshold: 70mA
3h: Slew rate: 15V/µs	Current limit: 75mA	Overcurrent threshold: 53mA

5.8.6 SIO1 (0x23)

This register controls the IO-Link-channel (channel1) if it is configured in SIO mode. Please note the inverted logic!

Bit	7	6	5	4	3	2	1	0
Name	reserved						IN	OUT
Access	-						R	R/W
Default	-						0	0

Table 21 – SIO1 register

OUT *CQ1* *Driver Output Value*

0b Set CQ1 to high level
1b Set CQ1 to low level

IN *Status of Pin CQ1*

0b Pin CQ1 is at high level
1b Pin CQ1 is at low level

5.8.7 SIO2 (0x43)

This register controls the output and can read the input at channel2. Please note the inverted logic!

Bit	7	6	5	4	3	2	1	0
Name	reserved						IN	OUT
Access	-						R	R/W
Default	-						0	0

Table 22 - SIO2 register

OUT *DIO Driver Output Value*

0b Set DIO to high level
1b Set DIO to low level

IN *Status of Pin DIO*

0b Pin DIO is at high level
1b Pin DIO is at low level

5.8.8 UART (0x24)

If channel1 is configured in UART mode, reading this register returns a received UART character. Writing to this register sends the given character using the integrated UART.

Bit	7	6	5	4	3	2	1	0
Name	DATA (UART_TX write / UART_RX read)							
Access	R/W							
Default	00h							

Table 23 - UART register

DATA *UART character*

5.8.9 FHC (0x25)

This register is used to configure and control the behavior of the frame handler (IO-Link mode) of channel1.

Bit	7	6	5	4	3	2	1	0
Name	RST	SKIP	reserved					TOUT
Access	W	W	-					R/W
Default	0	0	00h					0

Table 24 – FHC register

TOUT *Use relaxed timeout watchdog (+3T_{BIT})*

SKIP *Skip current frame (**Note**: while writing to this bit, other register values won't be changed)*

RST *Reset frame handler (**Note**: while writing to this bit, other register values won't be changed)*

5.8.10 ODL (0x26)

This register configures the length of the on-request data in bytes. According to the IO-Link specification, valid values are 1, 2, 8 or 32. (**Note**: Writing to this register causes a reset of the framehandler.)

Bit	7	6	5	4	3	2	1	0
Name	LEN							
Access	R/W							
Default	01h							

Table 25 - ODL register

LEN *On-Request Data Length*

5.8.11 MPDL (0x27)

This register configures the length of the master process data in bytes. Valid values are 0-32. (**Note**: Writing to this register causes a reset of the framehandler.)

Bit	7	6	5	4	3	2	1	0
Name	LEN							
Access	R/W							
Default	00h							

Table 26 - MPDL register

LEN *Master Process Data Length*

5.8.12 DPDL (0x28)

This register configures the length of the device process data in bytes. Valid values are 0-32. (**Note**: Writing to this register causes a reset of the framehandler.)

Bit	7	6	5	4	3	2	1	0
Name	LEN							
Access	R/W							
Default	00h							

Table 27 - DPDL register

LEN *Device Process Data Length*

5.8.13 BLVL (0x29)

This register returns the current fill level of the frame handlers input buffer. This can be used for bulk access to the FHD register.

Bit	7	6	5	4	3	2	1	0
Name	FCNT							
Access	R							
Default	00h							

Table 28 - BLVL register

FCNT *Fill count of the frame handlers input buffer*

5.8.14 FHD (0x2A)

If channel1 is configured in IO-Link mode, reading this register returns the buffered UART characters of a received message. Writing to this register buffers the given characters for an outgoing message (via a ringbuffer), which gets sent over the integrated UART.

Bit	7	6	5	4	3	2	1	0
Name	DATA							
Access	R/W							
Default	-							

Table 29 - FHD register

DATA *Message character*

Depth of buffer: 66 Byte.

5.8.15 TRSH (0x2E)

This register is used to set a threshold level which is used for level interrupt triggering. (see 5.8.25)

Bit	7	6	5	4	3	2	1	0
Name	reserved		LVL					
Access	-		R/W					
Default	-		00h					

Table 30 - TRSH register

LVL *Threshold for level interrupt triggering (after TLVL received characters)*

5.8.16 REV (0x60)

This register contains the CCE4502 revision code.

Bit	7	6	5	4	3	2	1	0
Name	MAJ				MIN			
Access	R				R			
Default	1100b				1100b			

Table 31 - REV register

MAJ *Major revision code*

MIN *Minor revision code*

5.8.17 PROT (0x61)

This channel protection register controls if the IO-Link channel should become disabled by on chip high temperature or high VCC voltage protection. (**NOTE**: disabling this function may cause damage to master and/or device)

Bit	7	6	5	4	3	2	1	0
Name	reserved					PTEMP	PVCCH	reserved
Access	-					R/W	R/W	-
Default	-					1b	1b	-

Table 32 - PROT register

PTEMP *Channel disable on over temperature*

0b Channel is not disabled if over-temperature was flagged
1b Channel is disabled if over-temperature was flagged

PVCCH *Channel disable on over voltage*

0b	Channel is not disabled if over-voltage was flagged
1b	Channel is disabled if over-voltage was flagged

5.8.18 STAT (0x62)

This register contains some status information depending on the current mode that channel 1 is in.

Mode	Bit	7	6	5	4	3	2	1	0
SIO		reserved				WURQ	RXD	OUT2	OUT1
UART						OFLW	RXERR	RXRDY	TXRDY
FH						TOUT	STATE		
Access						R	R	R	R
Default						0	x	0	0

Table 33 - STAT register

OUT1 Channel output value

0b CQ1 is driven high
1b CQ1 is driven low

OUT2 Channel output value

0b DIO is driven high
1b DIO is driven low

RXD Input state

0b High level detected at input CQ1
1b Low level detected at input CQ1

WURQ Wakeup request received

0b No wakeup request (IO-Link) received
1b Wakeup request (IO-Link) received

TXRDY UART Transmit state

0b UART is busy transmitting
1b UART is ready to send

RXRDY UART receive state

0b UART is ready to receive new data
1b New Data is available in UART

RXERR UART parity error flag

0b Last byte was received without parity error
1b Last byte received with parity error

OFLW UART receive buffer overflow

0b No receive buffer overflow
1b UART received byte, but receive buffer was not empty

STATE Frame Handler state

000b IDLE
001b Transmission output required
010b Transmission active; no further output required
011b Transmission active; further output required
100b Receiving active
101b Receiving active; new input available
110b Receiving active; message erroneous

111b Receiving active; message erroneous; new input available

TOUT *Frame handler timeout (after 25 T_{BIT})*

0b No timeout detected
1b Timeout detected

5.8.19 INT_SRC_STAT (0x63)

The status interrupt-source-register contains various relevant status information of the IC. All bits are set by hardware. An interrupt is generated if at least one of these bits is enabled via INT_EN_STAT and contains a '1'. Writing a '1' to either of these bits clears this interrupt-source individually. Writing a '0' to any of these bits has no effect.

Bit	7	6	5	4	3	2	1	0
Name	reserved	HIGH_T	HIGH_VS	Reserved	CH_DIS2	CH_DIS1	SD2	SD1
Access	-	R/W1	R/W1	-	R/W1	R/W1	R/W1	R/W1
Default	-	0	0	-	0	0	0	0

Table 34 - INT_SRC_STAT register

SD1/2 *Short detected at pin CQ1 and DIO*

CH_DIS1/2 *Channel CQ1 and DIO disabled due to a detected overload*

HIGH_VS *High voltage detected*

HIGH_T *High temperature detected*

5.8.20 INT_EN_STAT (0x64)

The status interrupt-enable-register allows the user to enable each status interrupt-source individually.

Bit	7	6	5	4	3	2	1	0
Name	-	HIGH_T_EN	HIGH_VS_EN	-	CH_DIS2_EN	CH_DIS1_EN	SD2_EN	SD1_EN
Access	-	R/W	R/W	-	R/W	R/W	R/W	R/W
Default	-	0	0	-	0	0	0	0

Table 35 - INT_EN_STAT register

SD1/2_EN *Enables the interrupt source SD* *(0b: disabled 1b: enabled)*

CH_DIS1/2_EN *Enables the interrupt source CH_DIS* *(0b: disabled 1b: enabled)*

HIGH_VS_EN *Enables the interrupt source HIGH_VS* *(0b: disabled 1b: enabled)*

HIGH_T_EN *Enables the interrupt source HIGH_T* *(0b: disabled 1b: enabled)*

5.8.21 INT_SRC_SIO (0x65)

The SIO interrupt-source-register contains all relevant information of the SIO-mode. All bits are set by hardware. An interrupt is generated if at least one of these bits is enabled via INT_EN_SIO and contains a '1'. Writing a '1' to either of these bits clears this interrupt-source individually. Writing a '0' to any of these bits has no effect.

Bit	7	6	5	4	3	2	1	0
Name	reserved					WURQ	CQ1_FALL	CQ1_RISE
Access	-					R/W1	R/W1	R/W1
Default	-					0	0	0

Table 36 - INT_SRC_SIO register

CQ1_RISE *Rising edge at Pin CQ1 (voltage changes from 0V to VS)*

CQ1_FALL *Falling edge at Pin CQ1 (voltage changes from VS to 0V)*

WURQ *Wakeup Request detected*

5.8.22 INT_EN_SIO (0x66)

The SIO interrupt-enable-register allows the user to enable each SIO interrupt-source individually.

Bit	7	6	5	4	3	2	1	0
Name	reserved					WURQ_EN	CQ1_FALL_EN	CQ1_RISE_EN
Access	-					R/W	R/W	R/W
Default	-					0	0	0

Table 37 - INT_EN_SIO register

CQ1_RISE_EN *Enables the interrupt source CQ1_RISE* *(0b: disabled 1b: enabled)*

CQ1_FALL_EN *Enables the interrupt source CQ1_FALL* *(0b: disabled 1b: enabled)*

WURQ_EN *Enables the interrupt source WURQ* *(0b: disabled 1b: enabled)*

5.8.23 INT_SRC_UART (0x67)

The UART interrupt-source-register contains all relevant information of the UART-mode. All bits are set by hardware. An interrupt is generated if at least one of these bits is enabled via INT_EN_SIO and contains a '1'. Writing a '1' to either of these bits clears this interrupt-source individually. Writing a '0' to any of these bits has no effect.

Bit	7	6	5	4	3	2	1	0
Name	reserved					RX_OVFLW	RX_REC	TX_RDY
Access	-					R/W1	R/W1	R/W1
Default	-					0	0	0

Table 38 - INT_SRC_UART register

TX_RDY *UART is ready to send data. Data can be written to UART (0x24)*

RX_REC *UART received one octet. Received data can be fetched from UART (0x24)*

RX_OVFLW *UART receive overflow*

5.8.24 INT_EN_UART (0x68)

The UART interrupt-enable-register allows the user to enable each UART interrupt-source individually.

Bit	7	6	5	4	3	2	1	0
Name	reserved					RX_OVFLW_EN	RX_REC_EN	TX_RDY_EN
Access	-					R/W	R/W	R/W
Default	-					0	0	0

Table 39 - INT_EN_UART register

TX_RDY_EN *Enables the interrupt source TX_RDY* *(0b: disabled 1b: enabled)*

RX_REC_EN *Enables the interrupt source RX_REC* *(0b: disabled 1b: enabled)*

RX_OVFLW_EN *Enables the interrupt source RX_OVFLW* *(0b: disabled 1b: enabled)*

5.8.25 INT_SRC_FH (0x69)

The FH interrupt-source-register contains all relevant information of the framehandler-mode. All bits are set by hardware. An interrupt is generated if at least one of these bits is enabled via INT_EN_FH and contains a '1'. Writing a '1' to either of these bits clears this interrupt-source individually. Writing a '0' to any of these bits has no effect.

Bit	7	6	5	4	3	2	1	0
Name	reserved			TOUT	SOT	SOR	LVL	MSG
Access	-			R/W1	R/W1	R/W1	R/W1	R/W1
Default	-			0	0	0	0	0

Table 40 - INT_SRC_FH register

MSG *End of Message (Triggers after the last character of a message was received)*

LVL *Message Level (Triggers if a defined amount of buffered characters is reached, see 5.8.15)*

SOR *Start of Receiving (Triggers as soon as the device starts receiving a message)*

SOT *Start of Transmitting (Triggers when the device starts transmitting its message)*

TOUT *Timeout detected*

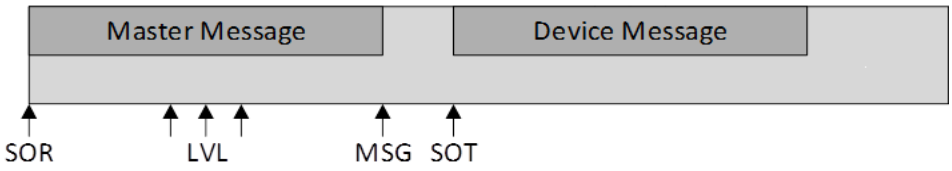


Figure 11 - Interrupt Trigger Positions

5.8.26 INT_EN_FH (0x6A)

The FH interrupt-enable-register allows the user to enable each FH interrupt-source individually.

Bit	7	6	5	4	3	2	1	0
Name	reserved			TOUT_EN	SOT_EN	SOR_EN	LVL_EN	MSG_EN
Access	-			R/W	R/W	R/W	R/W	R/W
Default	-			0	0	0	0	0

Table 41 - INT_EN_FH register

MSG_EN	*Enables the interrupt source MSG*	*(0b: disabled*	*1b: enabled)*
LVL_EN	*Enables the interrupt source LVL*	*(0b: disabled*	*1b: enabled)*
SOR_EN	*Enables the interrupt source SOR*	*(0b: disabled*	*1b: enabled)*
SOT_EN	*Enables the interrupt source SOT*	*(0b: disabled*	*1b: enabled)*
TOUT_EN	*Enables the interrupt source TOUT*	*(0b: disabled*	*1b: enabled)*

5.8.27 CLK_OUT (0x6C)

This register controls the clock output of the chip. If the clock is not externally needed, the output pad for port CLK_EXT can be disabled via bit CLK_OUT_DIS.

Bit	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
Name	reserved							CLK_OUT_DIS
Access	-							R/W
Default	-							0b

table 42 : CLK_OUT register

CLK_OUT_DIS *Output Clock disable*

0b CLK_EXT is not disabled
1b CLK_EXT is disabled

5.9 INTERRUPT HANDLING

All interrupt-sources can be masked via their corresponding enable-register. All not masked interrupt-sources, which consist of the 4 irq-source registers (5.8.19, 5.8.21, 5.8.23, 5.8.25), are logically "or"ed and the result is inverted for the final output at the INTX-pin. The single interrupt sources get set to '1' in any case, no matter if the corresponding interrupt is enabled or not. The INTX-pin however only gets active ('0') if a source is also enabled by the corresponding enable-register. All interrupt sources must be cleared actively by the user (e.g. MCU) by writing a '1' to the specific bit. By default, all interrupt-sources are disabled at startup and need to be actively set by the user. Keep in mind that there is no global interrupt enable.

5.10 SPI (SERIAL PERIPHERAL INTERFACE)

5.10.1 Signal Description

Name	Type	Description
MOSI	Input	Data input
MISO	Output	Data output
SCLK	Input	Clock input (f_{MAX} = 20 MHz)
SSX	Input	Slave select (active-low)
INTX	Output	Interrupt output for microcontroller (active-low)

Table 43 - Signal Description

5.10.2 Data Format

The CCE4502 is configured as SPI slave and uses the CPOL=0, CPHA=0 configuration, i. e. SCLK is low in idle mode and the data has to be valid on the rising edge of SCLK. During each transaction, a minimum of 2 bytes has to be transferred. For bulk access to the frame-handler-buffer via the FHD register, n bytes can be transferred. The first received byte after a falling SSX edge always reflects the current status of the two channels. The format depends on the configured modes.

Figure 12 illustrates the timing of a SPI access and Table 44 contains the related timing characteristics.

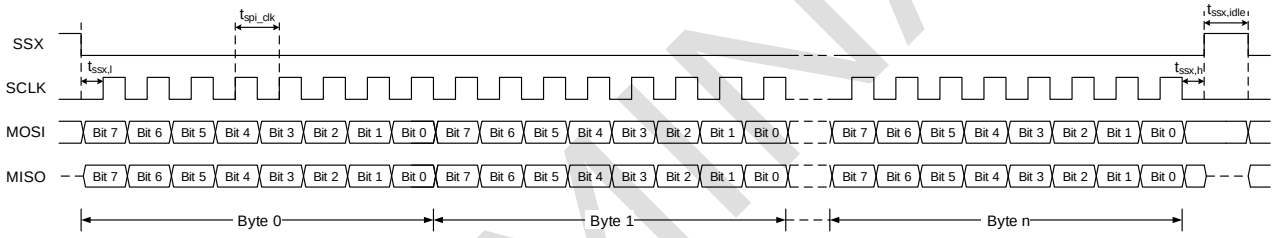


Figure 12 - SPI timing diagram

Characteristic	Symbol	Min.	Max.	Unit
SPI frequency	t_{spi_clk}		20	MHz
SSX high pulse	$t_{ssx,idle}$	70		ns
SSX low to SCLK high	$t_{ssx,l}$	35		ns
SCLK low to SSX high	$t_{ssx,h}$	35		ns

Table 44 - SPI timing characteristics

5.10.3 MOSI Format

Bit	7	6	5	4	3	2	1	0
1st Byte	ADR							R/W
2nd Byte	DATA							
	...							
nth Byte	DATA							

Table 45 - MOSI Format

ADR **Address for register access**

0x20-0x3F	Channel 1 registers
0x40-0x5F	Channel 2 registers
0x60-0x7F	Common registers

R/W **Register access type**

b0 write to address
b1 read from address

DATA ***Value for write access***
3rd – nth byte is optional; ignored on read access

5.10.4 MISO Format

Bit	7	6	5	4	3	2	1	0
1st Byte	STAT							
2nd Byte	DATA							
	...							
nth Byte	DATA							

Table 46 - MISO Format

STAT **status of the IC (see 5.10.5)**

DATA **Current value on read access to register**
3rd – nth byte is optional; not valid on write access

5.10.5 STAT Format

The IC uses the SPI status byte to indicate its current status. Depending on the mode, which is set in the CONF1 register (5.8.2), STAT changes its format.

Mode	Mode Name	7	6	5	4	3	2	1	0
0b00	SIO Mode	HIGH_T	HIGH_VS	-	WURQ	SD2	SD1	MODE	
0b01	UART Mode	HIGH_T	RX_ERR	RX_RDY	TX_RDY	SD2	SD1	MODE	
0b10	IO-Link Mode	TOUT	FH_STAT			SD2	SD1	MODE	

Table 47 - STAT Format

MODE *IC mode*

0h: SIO Mode (default)
1h: UART Mode
2h: IO-Link Mode
3h: reserved

SD1/SD2 *Short Detection on CQ1 and DIO*

WURQ *Wake-Up on CQ1 detected*

HIGH_VS *High voltage indicator*

HIGH_T *High temperature indicator*

TX_RDY *UART transmitter ready*

RX_RDY *UART receiver ready (input available)*

RX_ERR *UART parity error*

FH_STAT *Frame Handler state*

000b: IDLE
001b: Transmission output required

010b: Transmission active; no further output required
011b: Transmission active; further output required
100b: Receiving active
101b: Receiving active; new input available
110b: Receiving active; message erroneous
111b: Receiving active; message erroneous; new input available

TOUT *Frame handler timeout (after 25 T_{BIT})*

0b: No timeout detected
1b: Timeout detected

6 APPLICATION NOTES

6.1 POWER DISSIPATION CONSTRAINTS

The CCE4502 QFN24 package has a thermal resistance of 40 K/W from silicon junction to ambient with an optimized PCB design. With maximum ambient temperature of 105°C and maximum junction temperature of 150°C a maximum power dissipation of 1.125W can be handled by the thermal capabilities of the QFN package.

Following table gives an overview about the power contributions of the different circuit blocks contained in the CCE4502 and calculated at nominal condition $V(L_+)$ = 24V.

Circuit Block	Voltage Drop	Current	Power
IO Channel 1	2 V	200 mA	0.400 W
IO Channel 2	2 V	200 mA	0.400 W
5/3.3V Regulator (3.3V), Reference	5.2 V	50 mA	0,260 W
5V Regulator	19 V	10 mA	0.190 W
1.8V Regulator (internal)	8.5 V	3 mA	0.025 W
DC/DC Converter (in buck mode)	15.5 V	60 mA	0.186 W
DC/DC Converter (in linear mode)	15.5 V	60 mA	0.930 W

Table 48 CCE4502 Power contributions

The calculated power sum with nearly 1.4 Watt (DC/DC in buck mode) shows that tradeoffs must be made in the overall system design and by using the different features of the CCE4502 IC.

6.2 APPLICATION WITH DC/DC CONVERTER IN BUCK MODE

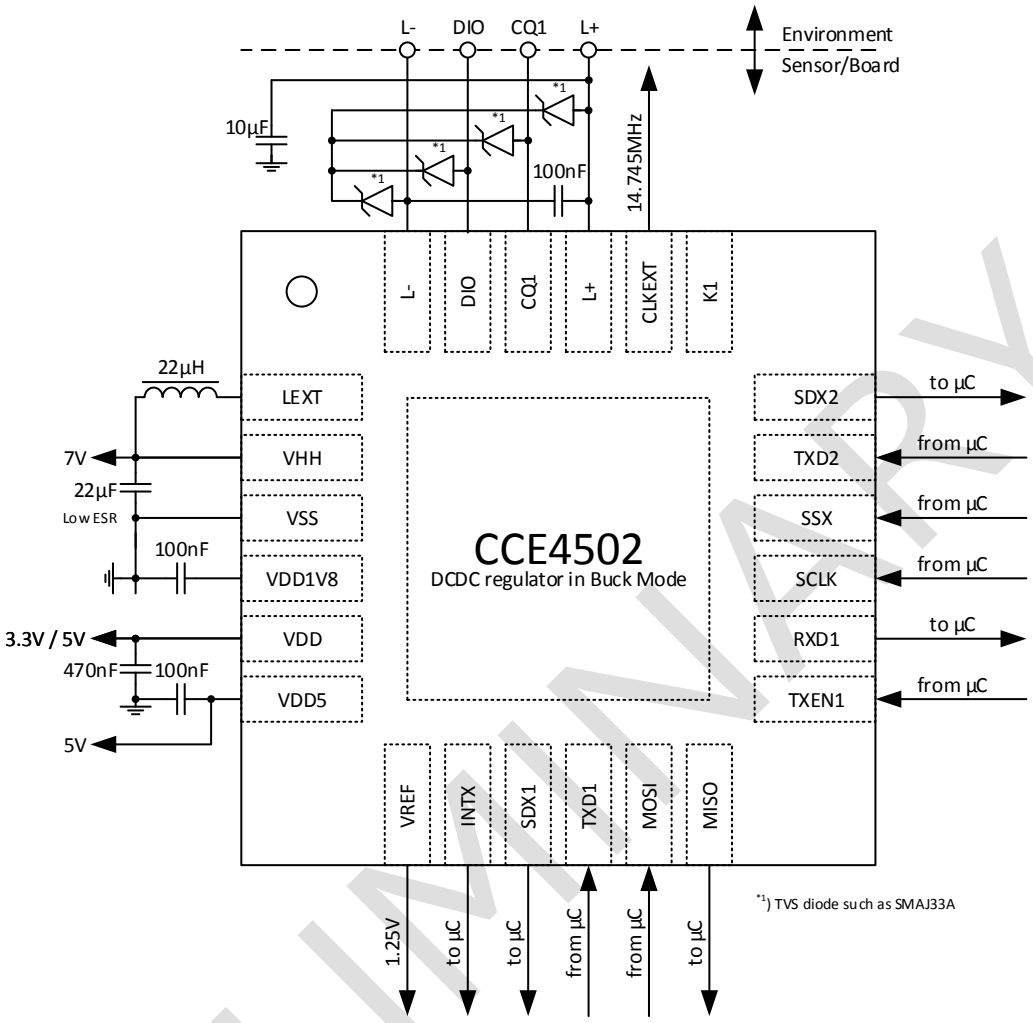


Figure 13 - Application with active DC/DC Converter (Supply Mode 1)

6.3 APPLICATION WITH DC/DC CONVERTER IN LINEAR MODE

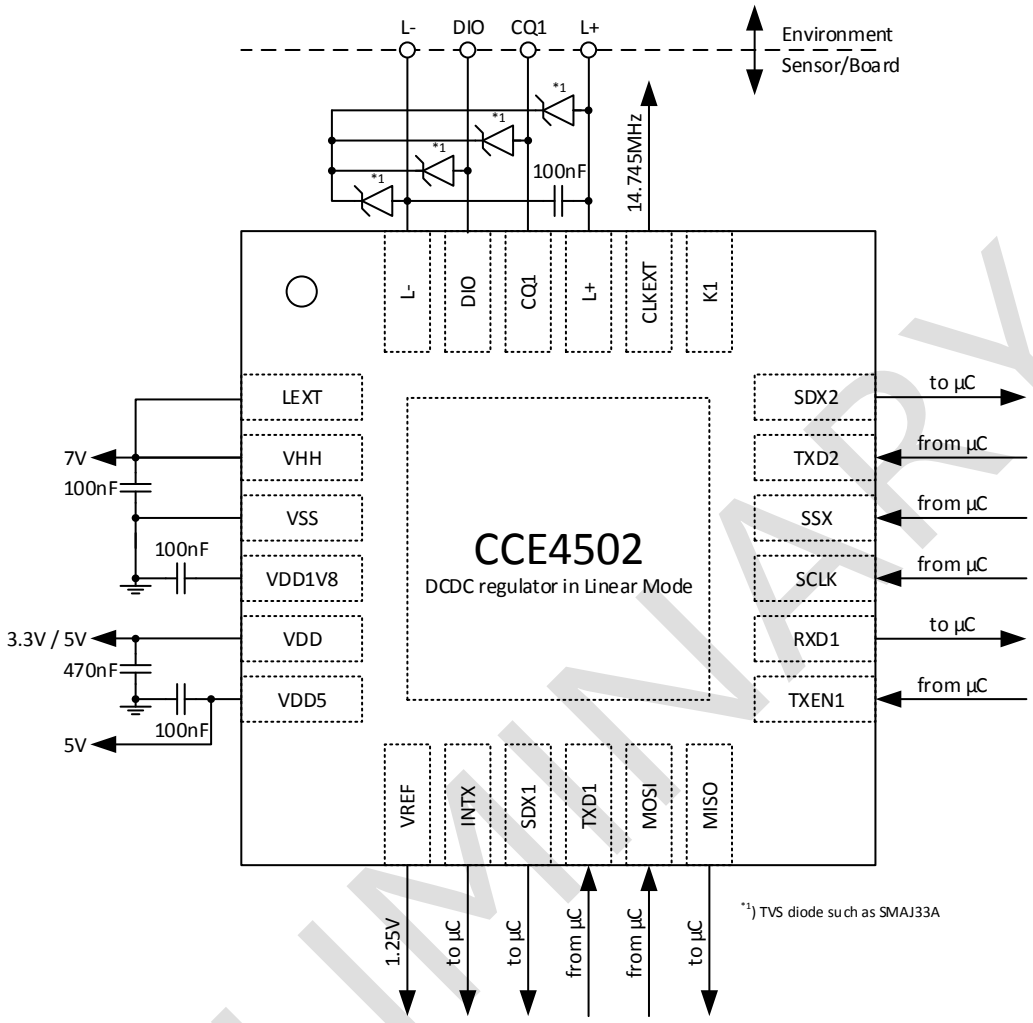


Figure 14 - Application with disabled DC/DC Converter (Supply Mode 2)

6.4 APPLICATION WITH EXTERNAL SUPPLY

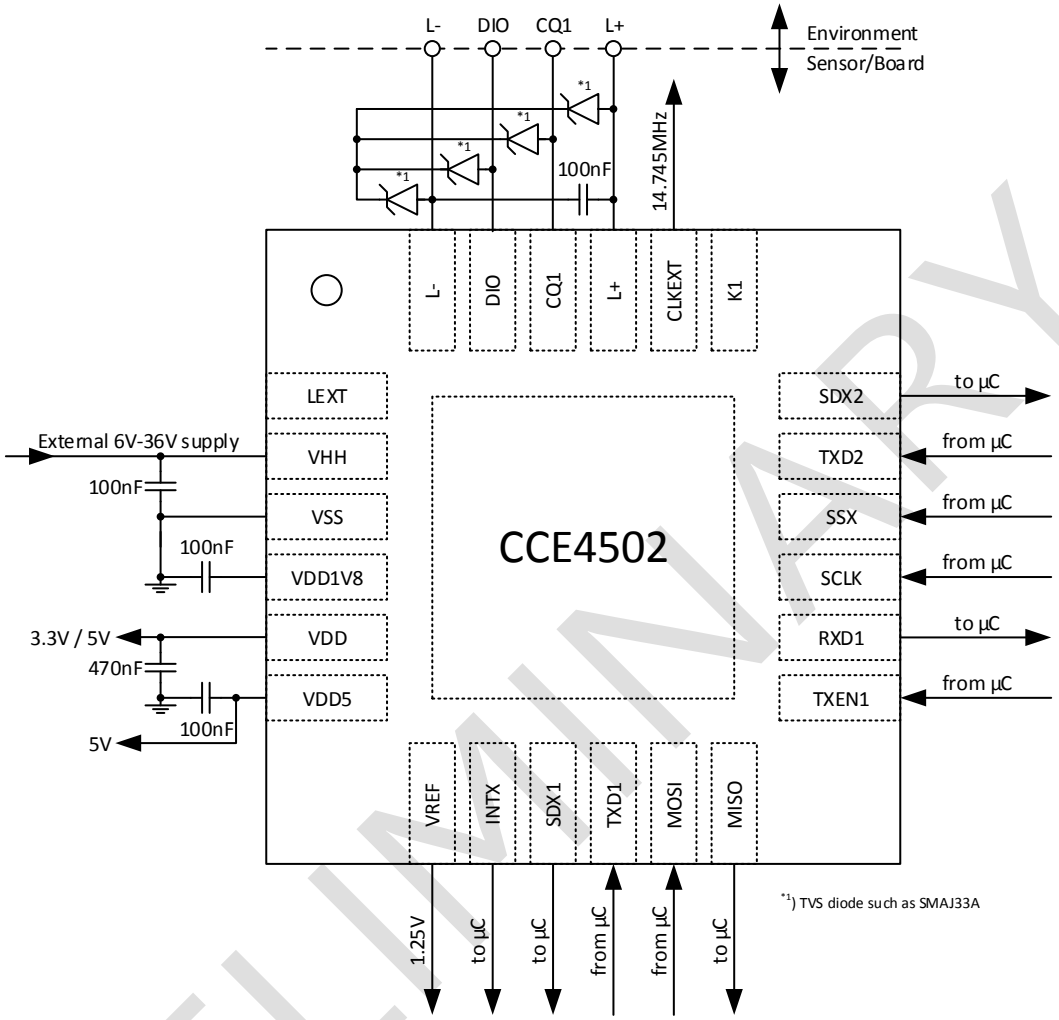


Figure 15 - Application with external supply (Supply Mode 3)

7 PACKAGE OUTLINE

7.1 QFN24 PACKAGE

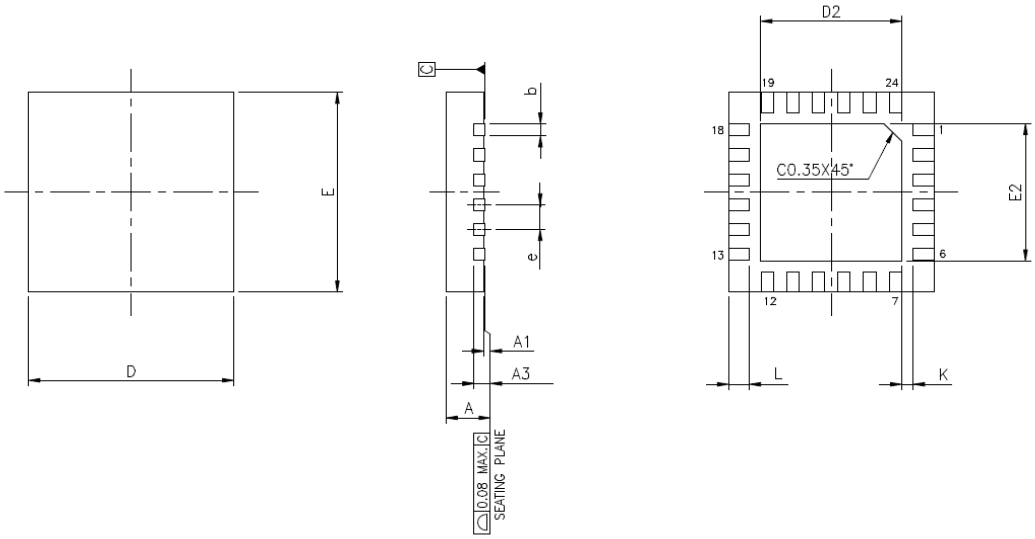


Figure 16 - QFN24 Package

Symbol	A	A1	A3	b	D	E	e	L	K	D2	E2
Min	0.70	0.00	0.20 REF.	0.18	4.00 BSC.	4.00 BSC.	0.50 BSC.	0.35	0.20	2.50	2.50
Typ	0.75	0.02		0.25				0.40	-	2.60	2.60
Max	0.80	0.05		0.30				0.45	-	2.65	2.65

UNIT : mm

NOTES :

1. JEDEC OUTLINE : MO-220 WGGD-6.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. THE MINIMUM "K" VALUE OF 0.20mm APPLIES.
4. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

7.2 CHIP SCALE PACKAGE (BUMPED DIE)

A Chip Scaled Package (CSP) is provided on request. Figure 17 show the die and bump configuration.

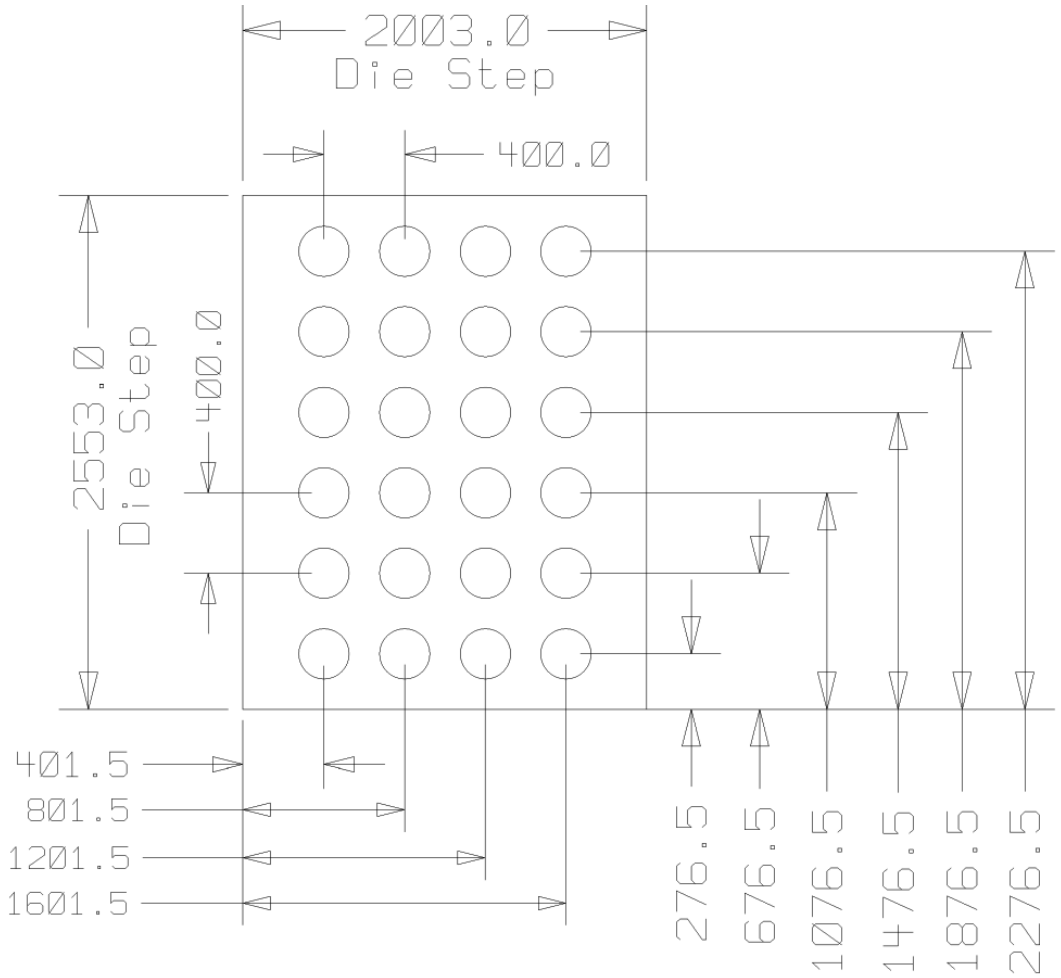


Figure 17 - CSP die and bump position

8 TAPE AND REEL INFORMATION

8.1 TAPE QFN24 PACKAGE

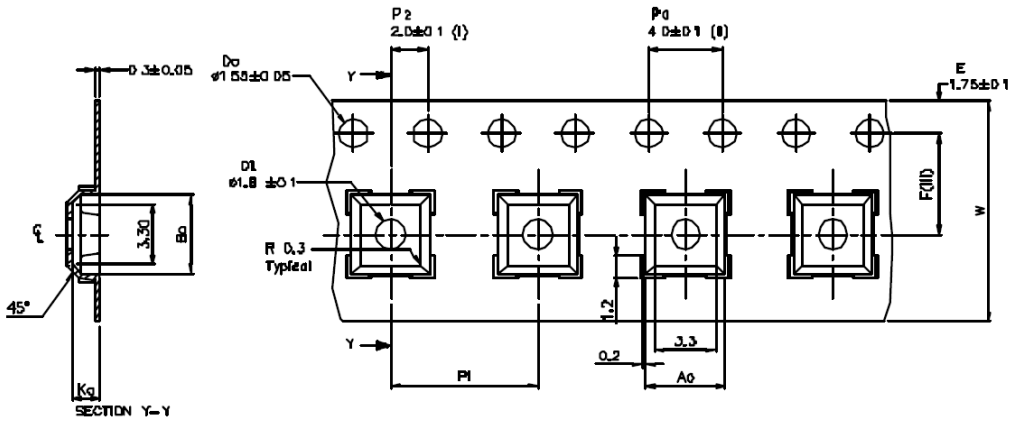


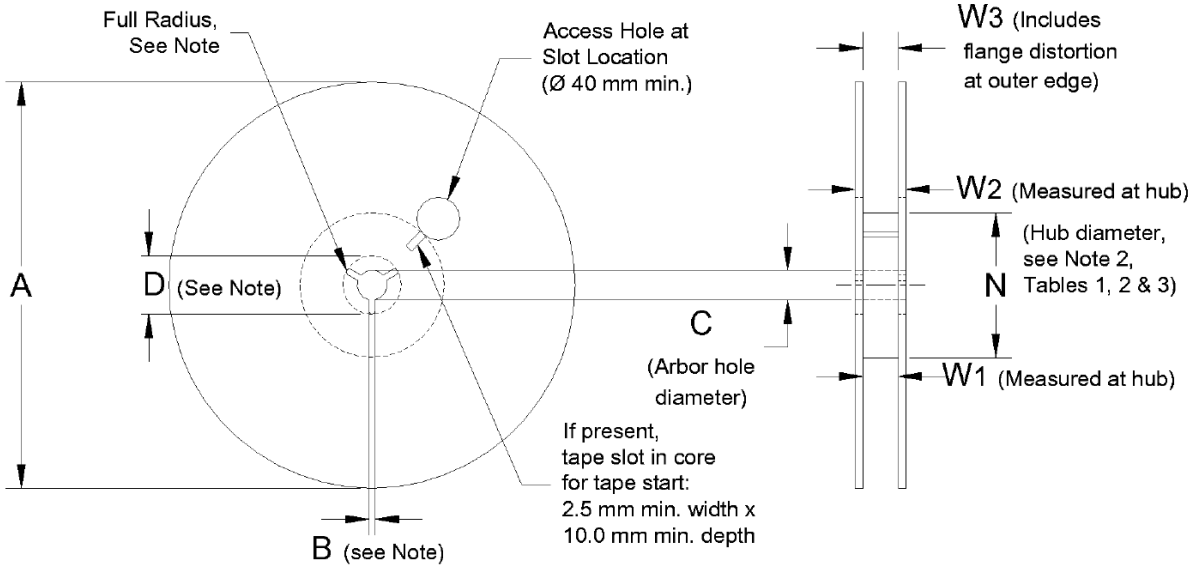
Figure 18 - Tape Dimensions

Ao	4.30 +/– 0.1
Bo	4.30 +/– 0.1
Ko	1.50 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

8.2 REEL INFORMATION



Note: Drive spokes optional; if used, dimensions B and D shall apply.

Figure 19 - Reel Dimensions

Symbol	A	B	C	D	W_1 QFN24
Min	-	1.5	12.8	20.2	13.25
Typ	-	-	13.0	-	-
Max	330	-	13.5	-	13.75

9 ORDERING INFORMATION

Parts are available as 5V or 3.3V output voltage VDD option with either Buck mode or linear mode DC/DC converter function. Please take the corresponding order no. from Table 49 and contact info@creativechips.com for an individual quote.

Part	Order No.	VDD Option	DC/DC Converter	Delivery	Quantity
CCE4502	CCE4502B5V	5V	Buck Mode	Tape & Reel	4.000
CCE4502	CCE4502B3.3V	3.3V	Buck Mode	Tape & Reel	4.000
CCE4502	CCE4502L5V	5V	Linear Mode	Tape & Reel	4.000
CCE4502	CCE4502L3.3V	3.3V	Linear Mode	Tape & Reel	4.000

Table 49 - Order codes

10 REVISION HISTORY

Revision	Date	Author	Description
1.0	01.03.2016	sl	First version
1.1	23.03.2016	dw	Introducing changes from NXP suggestions, slew rate control, etc.
	30.03.2016	SZ	Add power supply section, fixed application drawings
	31.03.2016	SZ	Added HV-output stage, Power On Reset sections, Fixed Parameter tables
1.2	21.04.2016	RBe	Updated IO-Link message types
	22.04.2016	RBe	Completely reworked the register interface (5.7)
	03.05.2016	SZ	Completed HV-IO description.
	03.05.2016	RBe	Renamed HV-ports (QIN_x --> TXDx; QENX_1 -->TXEN1; HL_1 -->RXD1)
	04.05.2016	SZ	Fixed pin description.
	04.05.2016	RBe	Added section 5.6 (Operational Modes) Updated section 5.8 (SPI)
1.3	10.05.2016	RSt	Corrected typing errors
	11.05.2016	RSt	Described CPOL/CPHA of SPI, Added reference to SLEW1/2 registers in elec. characteristics
	17.03.2016	RSt	Specified UART data width and parity
	18.03.2016	dw	Modified PSRR specification in Table 4
	19.05.2016	RSt	Corrected pins in Table 9
	24.05.2016	dw	Separate 5V regulator Reference voltage output DC/DC enabling/disabling over fuse array Modified pin arrangement Configuration pin modified Revision register / logic description Specification application note and power constraints Specify electrical characteristics for operating temperature range
	25.05.2016	SZ	Fixed OVLD1/2 register description Fixed CLKEXT function in application schematics and caption Moved Protection Circuit to Functional Description Fixed VHH absolute maximum rating Fixed external buck converter component values Reworked DC/DC converter description Added order codes for Buck Mode and Linear Mode of DC/DC converter Added Temperature sensor to Protection Circuitry figure Fixed power on reset drawing Fixed HV-Output stage logic drawing
1.4	26.05.2016	SZ	Reworked power supply description, Added 5V LDO and VREF output Addition of DC/DC parameter in Linear mode
	31.05.2016	RBe	Renamed Bit “IO” of SIO-reg and logic core port to “IN” Changed initial value of bits “ADIS” of reg OVLD1/2 Added Input to channel 2 in register SIO2 Added bit “DIS” to registers CONF2

	06.06.2016	DW	STAT byte format (5.9.5) approved
	10.06.2016	RBe	Fixed several typos Minor description changes for some registers
	20.06.2016	DW	VDD5 regulator can provide 10mA Removed few tbd's for regulators Insert CSP outline description
1.5	28.06.2016	DW	Removed last tbd's Specify deglitch time for overvoltage and -temperature flags
1.6	05.08.2016	SZ	Add CSP Pinout Start Up time relative to V_{L+} Fixed spelling.
	16.08.2016	RSt	Updated SPI STAT format description of IO Link mode
1.7	17.08.2016	SZ	Fixed power supply drawing
	23.08.2016	RBe	Added CLK_OUT register
	30.08.2016	RBe	Switched SD1 and SD2 in SPI status byte
	31.08.2016	RSt	Specified SPI timing characteristics
	01.09.2016	SZ	Abs. max. supply voltage to +-40V
	02.09.2016	SZ	Fixed Digital Input voltage thresholds
	02.09.2016	RSt	Corrected initial value of register FHD
1.8	12.09.2016	RSt/SZ	Removed references to revisions 1.7.x
	12.09.2016	SZ	Fixed maximum output current rating in 5V-LDO description
	12.09.2016	DW	Increase minimum blocking capacitor for programmable regulator 3.3/5V
	14.09.2016	RBe	Removed references to undervoltage detection
	22.09.2016	RBe	Added section for Interrupt Handling
	30.09.2016	DW	Change Pin name CQ2 to DIO
1.9	19.10.2016	AS	Updated Block Diagram
	21.10.2016	RSt	Removed references to undervoltage protection Fixed DIO replacement in QFN24 pinout
	27.10.2016	RSt	Fixed TXD spelling in QFN24 pinout
	28.10.2016	SZ	Preliminary watermark.
1.10	28.10.2016	RSt	Fixed application figures: removed cap. label (SM1), corrected VHH (SM3)
1.11	08.11.2016	RSt	Removed non-exisiting pins PN_1 and D_INV from block diagram
	11.11.2016	DW	Corrected pins of reference voltage to "7,3" in Table 3 Corrected names in VDD5 table (Table 5)
1.12	13.02.2017	RSt	IO-Link input level thresholds and pin numbers (Table 7) Modified document number
1.13	31.03.2017	RSt	Corrected TXD1 direction in application schematics

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