CREATIVE CHIPS GmbH

Data sheet
DD0085
Revision 1.0 / 1 February 2017

CCE4502 EvaBoard v1

IO-Link evaluation board

CREATIVECHIPS®
MICROELECTRONICS

CONTENTS

1 BOARD OVERVIEW

The CCE4502 EvaBoard v1 combines the CCE4502 device, an IO-Link™ compliant transceiver, with a Cypress® PSoC® 4000S microcontroller (MCU), two touch buttons (sensors), a temperature sensor and two LEDs as actors. Additionally, the board is equipped with a variety of connectors forming a basic platform for evaluation of the CCE4502 device.

A photography of the board is shown in Figure 1 and a block diagram is depicted in Figure 2.

Figure 1: Photography of the CCE4502 EvaBoard v1 (top view)

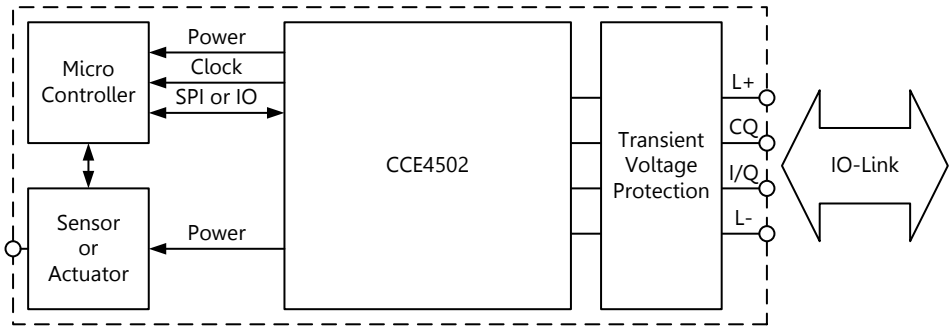

Figure 2: Block diagram

2 POWER SUPPLY

The CCE4502 EvaBoard is supplied via the L+ voltage of the IO-Link interface which has to be 24 V. The IO-Link interface comprises L+, L-, C/Q (CQ1) and I/Q (DIO), and it can be accessed via a M12 connector or terminal clamps. The CCE4502 device is directly connected to the IO-Link interface and comprises three voltage regulators. Four SMAJ33A TVS diodes are used to provide additional protection.

A regulated voltage of 7 V is generated at port VHH. Based on customer request, this regulator is factory programmed to operate either in DC/DC buck converter mode or in linear regulator mode. In buck converter mode it is capable of supplying up to 50 mA for external components. In linear regulator mode the load current is limited due to higher power dissipation of the used low-droput (LDO) regulator. In buck converter mode the pins 1 and 2 of jumper JP4 have to be shorted, otherwise pins 2 and 3 have to be shorted. See also Figure 3.

At port VDD a regulated voltage of 3.3 V or 5 V is generated by a LDO regulator. The voltage is based on customer request. This regulator supplies the digital I/O pads of the CCE4502, the MCU, the sensors and the actors. VDD can supply additional external components, but the overall combined external load of VHH and VDD must not exceed 50 mA. Please take into account that the current consumption of the MCU, the actors and the sensors has to be included in the 50 mA limit and can be up to 20 mA.

The port VDD5 is the output of a LDO regulator with a regulated voltage of 5 V. External components can be supplied by this port with a maximum load of 5 mA.

3 CCE4502

3.1 INTERFACES

All ports of the CCE4502 device, except LEXT and VDD1V8, are accessible on the CCE4502 EvaBoard. This provides full access to the feature set of the CCE4502. Figure 3 shows the connectors available on the board.

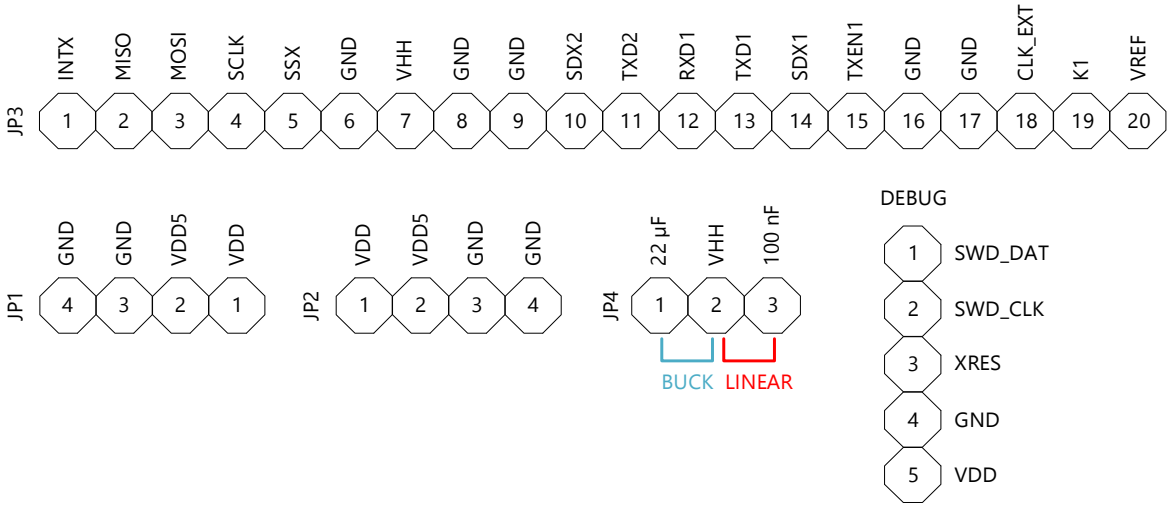

Figure 3: Connectors (without IO-Link connectors)

The SPI interface (SSX, SCLK, MOSI, MISO and INTX) of the CCE4502 device grants access to all registers of the CCE4502. Therefore all features of both IO-Link channels CQ1 and DIO can be enabled. The interface allows access to internal supervisor circuitry, such as the overtemperature detection, overvoltage detection and the output overcurrent protection. Furthermore on-chip logic, i. e. framehandler and wakeup detection, can be used to ease the IO-Link communication. This reduces the computation overhead for the microcontroller.

Besides SPI it is possible to control the outputs of CQ1 and DIO, and the input of CQ1 directly through the SIO ports of the CCE4502 device, i. e. RXD1, TXD1, TXD2 and TXEN1. The device is factory programmed to use these ports on both channels, thus it is possible to omit the SPI. Please note that when SPI is omitted all IO-Link protocol handling has to be performed by the MCU. However, this allows using the CCE4502 as a simple level shifter from 3.3V/5V logic signals to IO-Link compliant levels.

3.2 CLK_EXT CONFIGURATION

The CLK_EXT port is used as clock output port if port K1 is low. If port K1 is high it is used as clock input port. In clock output mode the clock of the calibrated internal oscillator is switched to CLK_EXT or CLK_EXT is floating, depending on the CLK_OUT register of the CCE4502. By default CLK_OUT is configured to disable the clock output. In clock input mode the logic core is clocked by the signal applied externally to CLK_EXT.

4 MICROCONTROLLER

The CCE4502 EvaBoard comprises a Cypress PsoC 4000S MCU in a QFN24 package. It can be used to control the CCE4502 device and it is required for controlling the on-board actors and sensors. The MCU can be removed on customer request. Without the MCU the on-board actors and sensors cannot be accessed.

4.1 INTERFACES

For programming and debugging of the MCU its SWD interface has to be used. It is accessible via the debug connector DEBUG. Please see the official programming specifications of the MCU vendor for further details.

The SPI interface and the SIO ports of the CCE4502 device are connected to GPIO ports of the MCU. See Table 1 for details.

The MCU can be reset via the debug connector DEBUG or by pressing the button SW1.

Table 1: MCU GPIO wiring

MCU GPIO port	Connected signal, function
P0.0	SSX
P0.1	INTX
P0.4	RXD1
P0.5	TXD1
P0.6	TXEN1
P1.2	Touch button 0
P1.3	Touch button 1
P1.7	SDX2
P2.0	LED “POWER”
P2.1	TXD2
P2.6	LED “STATUS”
P2.7	SDX1
P3.0	Temperature sensor DQ
P3.2	SWD_DAT (SWD interface)
P3.3	SWD_CLK (SWD interface)
P4.0	MOSI
P4.1	MISO
P4.2	SCLK

4.2 PERIPHERALS

There are two LEDs available as actors:

- a red LED (LED1, “POWER”) and
- a green LED (LED2, “STATUS”).

There are three sensors:

- two touch buttons (BTN0 and BTN1) and
- the temperature sensor Maxim Integrated DS18S20 which is a one wire digital thermometer.

All peripherals are connected to GPIO ports of the MCU and have to be controlled through the MCU. See Table 1 for details.

5 APPENDIX

5.1 SCHEMATIC AND LAYOUT

The following pages of this section contain the schematic and images of the layers of the board.

In the layout the symbol of the temperature sensor (IC3) is wrong. The Pins 1 and 3 are swapped. Therefore the device is assembled rotated by 180 degrees. Also in the layout the MCU is not connected to TXD1. The board is thus delivered with an additional wire connection on the board.

If the CCE4502 EvaBoard is configured to operate in VHH linear mode then L1 is replaced by a solder bridge.

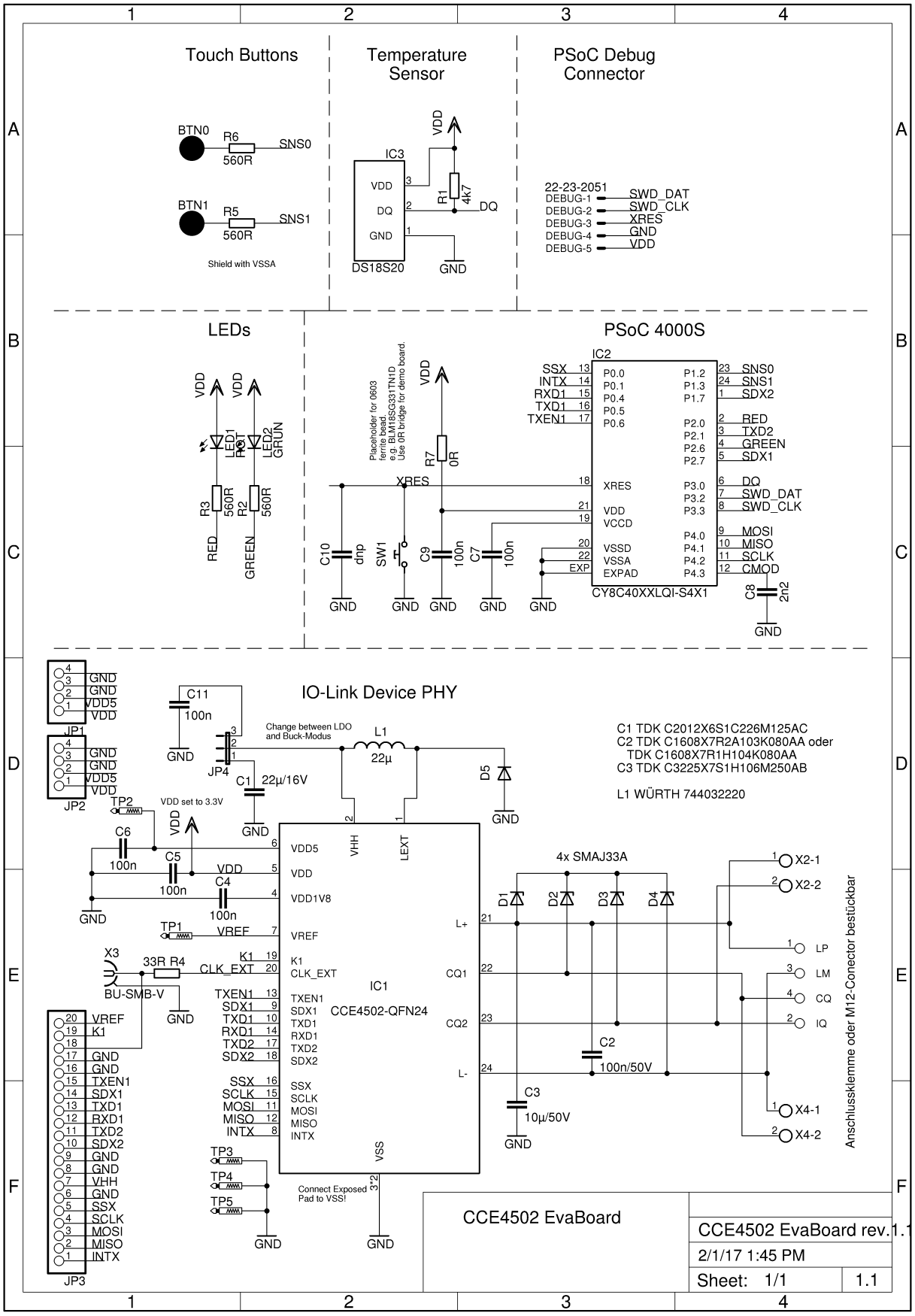

Figure 4: Schematic

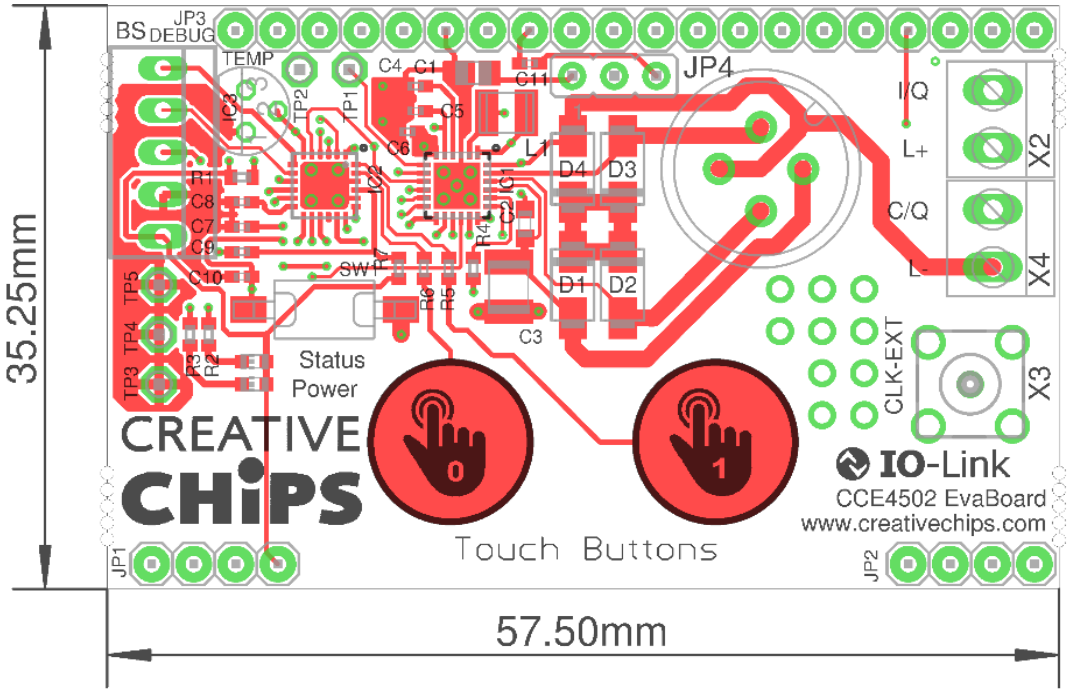

Figure 5: Layout top layer (viewed from top)

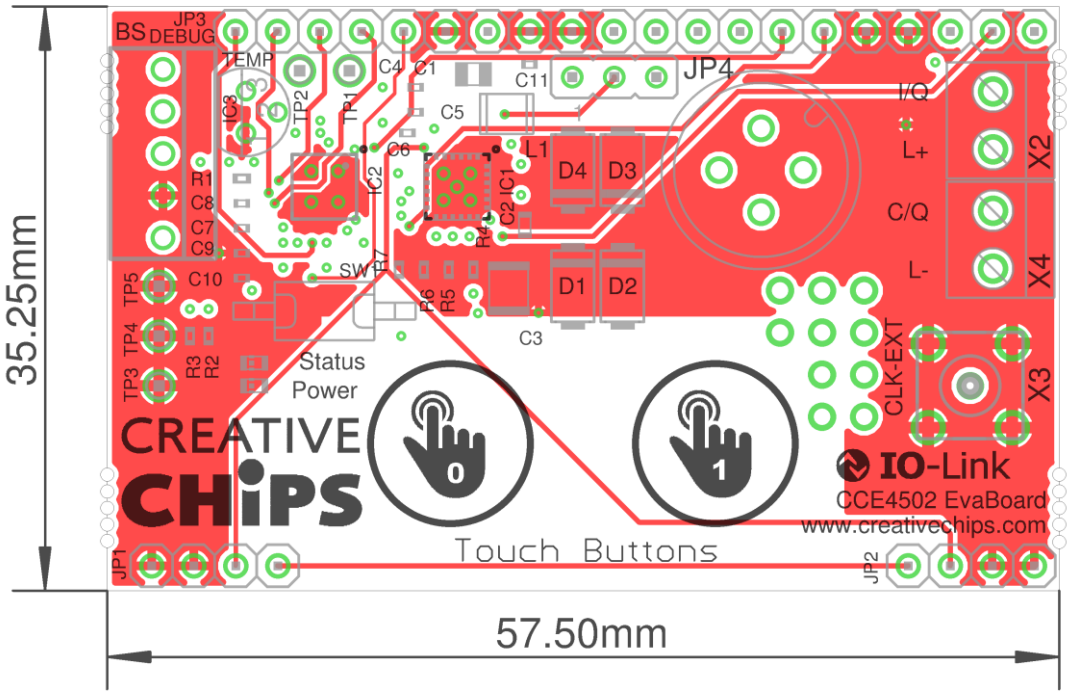

Figure 6: Layout middle layer 1 (viewed from top)

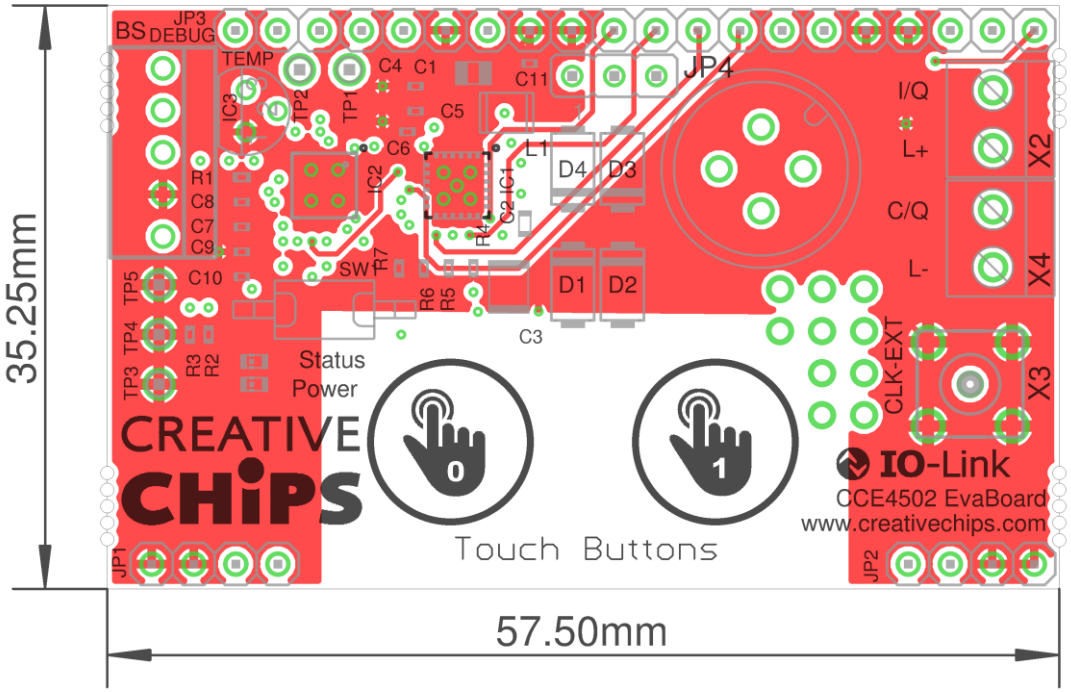

Figure 7: Layout middle layer 2 (viewed from top)

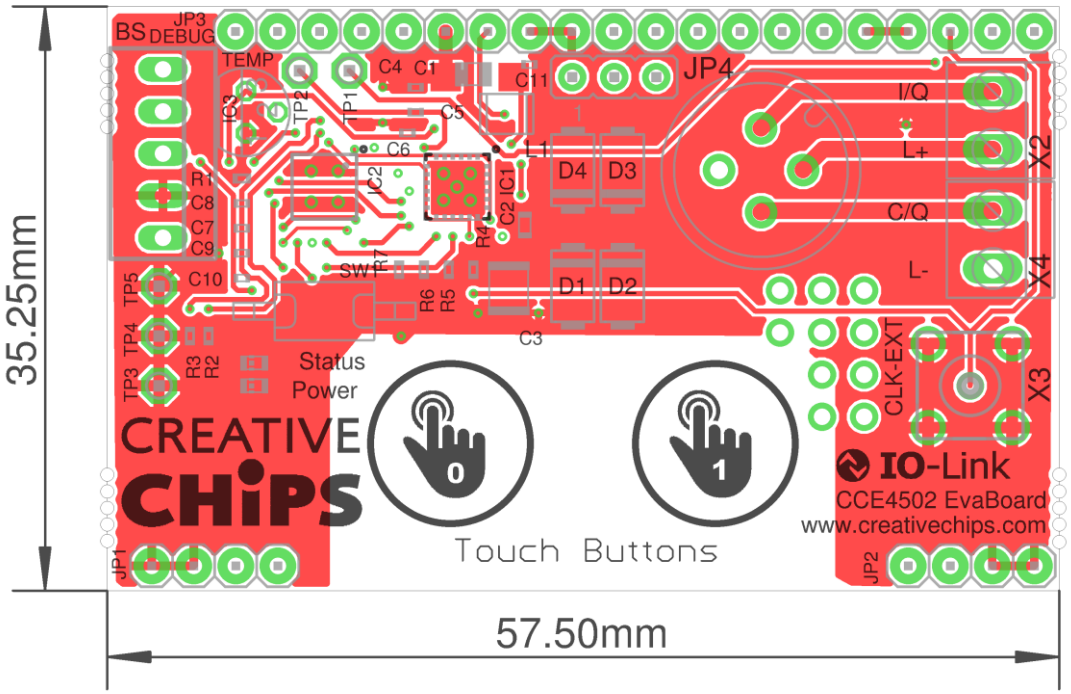

Figure 8: Layout bottom layer (viewed from top)

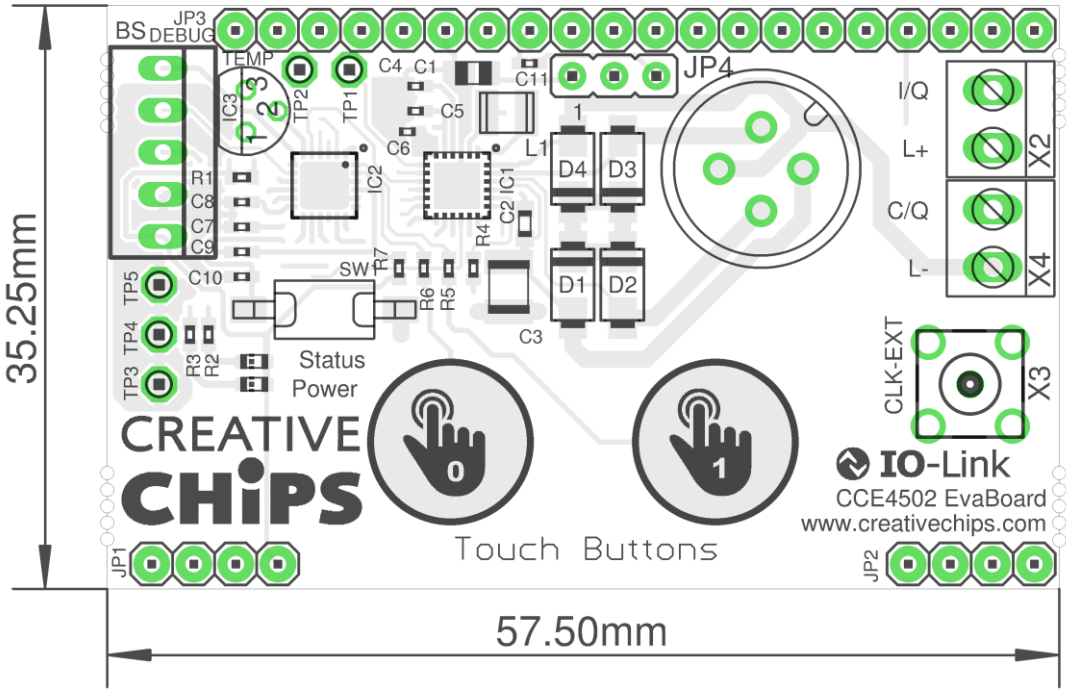

Figure 9: Assembly (viewed from top)

5.2 BILL OF MATERIALS

Table 2: Bill of materials

Part	Value
C1	22µF/16V
C2	100nF/50V
C3	10µF/50V
C4	100nF
C5	100nF
C6	100nF
C7	100nF
C8	2.2nF
C9	100nF
C10	dnp
C11	100nF
D1	SMAJ33A
D2	SMAJ33A
D3	SMAJ33A
D4	SMAJ33A
D5	1843668 / B340A-13-F B
DEBUG	Molex 22-23-2051
IC1	CCE4502-QFN24
IC2	CY8C4045LQI-S411
IC3	DS18S20
JP1	1x4 pin header
JP2	1x4 pin header
JP3	1x20 pin header
JP4	1x3 pin header
L1	22µH
LED1	red
LED2	green
R1	4k7 Ohms
R2	560R Ohms
R3	560R Ohms
R4	33R Ohms
R5	560R Ohms
R6	560R Ohms
R7	0R Ohms
SW1	SWITCH FSMSM
U$1	M12_CONNECTOR
X2	AKL 059-02
X3	SMB female connector for PCB
X4	AKL 059-02

6 REVISION HISTORY

Revision	Date	Author	Description
1.0	01.02.2017	AS, RSt	Initial version

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