1 GENERAL DESCRIPTION

High-voltage interface ASSP with overvoltage, high current and high temperature protection, based on a 0.35 µm HV-CMOS technology. Typical applications are industrial sensors or actuators. A variety in fields of application is given by different packaging and configuration options.

1.1 FEATURES

- One IO-Link compliant channel with up to 500 mA driving current (programmable P-mode, N-mode, push-pull)
- Additional high voltage output with same driving capabilities
- Integrated reverse-polarity protection
- DC/DC buck converter
- LDO voltage regulator (programmable as 3.3/5 V)
- Temperature compensated on-chip RC oscillator with ±2% frequency accuracy
- Overvoltage / high current protection
- High temperature detection
- Applicable as transceiver
- Integrated UART (COM1-3)
- Included frame handler (supports type 0, 1.1-1.2 and 2.1-2.6)
- SPI interface
- Various configuration options
- Evaluation board available

1.2 SCHEMATIC

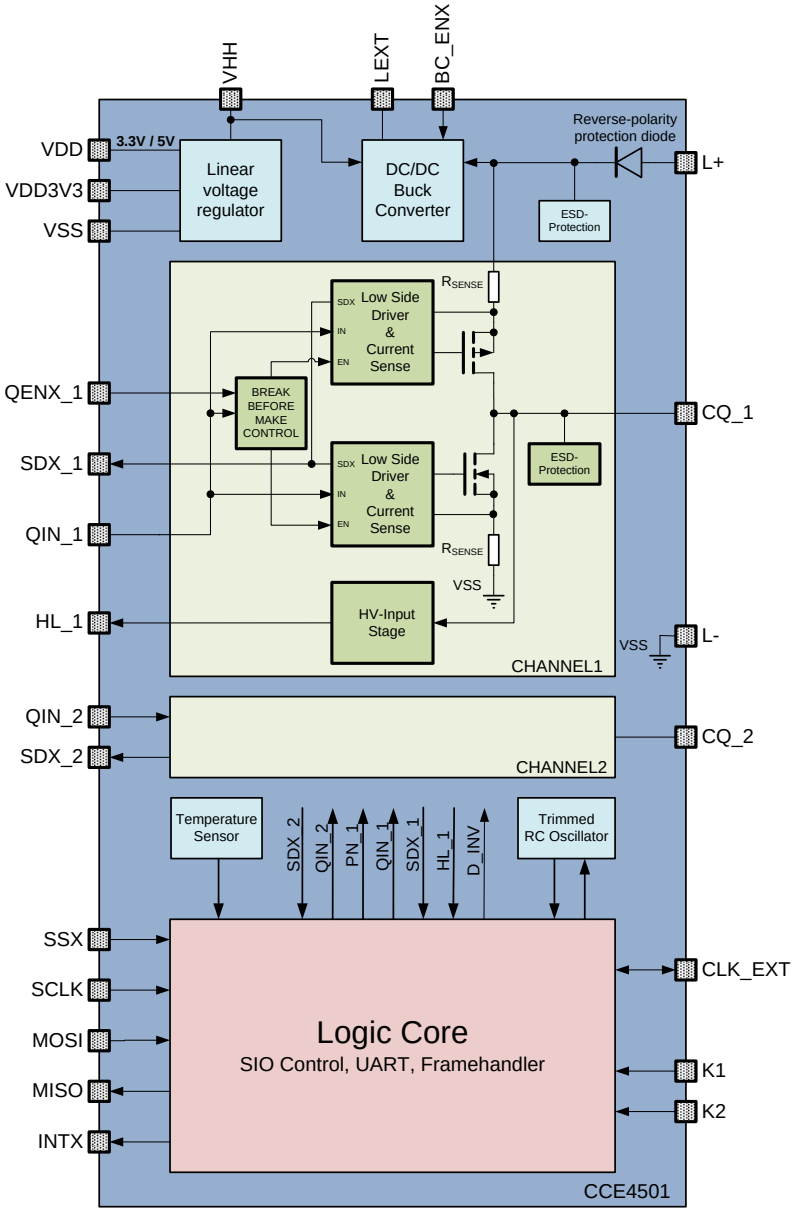


Figure 1 - Block Diagram

2 PINOUT

2.1 PACKAGE

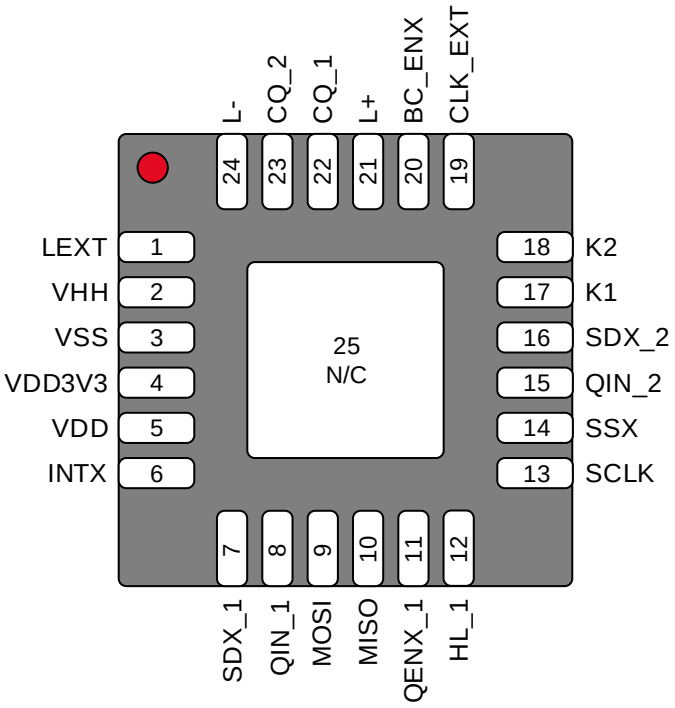


Figure 2 – QFN24 Package (4x4 mm)

2.2 PIN DESCRIPTIONS

Table 1 - Pin Descriptions

Pin No.	Name	Type	Function	Remarks
1	LEXT	PWR	External inductance	
2	VHH	PWR	Main supply / output DC/DC converter	
3	VSS	PWR	Ground (Signal)	
4	VDD3V3	PWR	3.3 V Supply Voltage Internal Logic	
5	VDD	PWR	3.3/5 V Supply Voltage Output	
6	INTX	OUT	Interrupt for micro controller	active-low
7	SDX_1	OUT	Channel 1 short detection	active-low
8	QIN_1	IN	Channel 1 signal input	
9	MOSI	IN	SPI Master Out/Slave In	100 kΩ pull down
10	MISO	OUT	SPI Master In/Slave Out	
11	QENX_1	IN	Channel 1 driver enable	active low, 100 kΩ pull up
12	HL_1	OUT	Channel 1 signal output	
13	SCLK	IN	SPI Clock	100 kΩ pull-down
14	SSX	IN	SPI Slave Select	100 kΩ pull-up
15	QIN_2	IN	Channel 2 signal input	
16	SDX_2	OUT	Channel 2 short detection	low active
17	K1	IN	Configuration bit 1	100 kΩ pull down

Pin No.	Name	Type	Function	Remarks
18	K2	IN	Configuration bit 1	100 kΩ pull down
19	CLK_EXT	IN/OUT	External clock input/Clock output	
20	BC_ENX	IN	DC/DC converter enable	active-low
21	L+	PWR	Positive supply (sensor)	
22	CQ_1	IN/OUT	IO-Link data channel 1	inverted logic
23	CQ_2	OUT	Switching output 2 (IO-Link compliant)	inverted logic
24	L-	PWR	Ground supply (Sensor)	

3 ABSOLUTE MAXIMUM RATINGS

T_{amb} = 25°C+/-1°C unless otherwise specified.

Table 2 - Absolut Maximum Ratings

Parameter	Conditions	Name	Min	Typ	Max	Unit
Supply Voltage	static	V_{L+} -V_{L-}	-0.7		36	V
Supply Voltage	dynamic (t <= 100ms)	V_{L+} -V_{L-_pulse}	-1		50	V
Power Dissipation	QFN24 Package on Multilayer PCB	P_{TOT}			1	W
Storage Temperature		$\vartheta_{storage}$	-55		155	°C
ESD Protection	Human Body model EIA/JESD22-A114-B	V_{ESD}	2			kV
Soldering Temperature	12 s max.	ϑ_{solder}			260	°C
FIT Rate					50	FIT
Junction Temperature		ϑ_{Junc}			150	°C

4 ELECTRICAL CHARACTERISTICS

T_{amb} = 25°C+/-1°C, V_{L+}-V_{L-} = 24 V unless otherwise specified.

4.1 GENERAL PARAMETERS

Table 3 - General Parameters

Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
Main Supply Voltage		21, 24	V_{L+} -V_{L-}	9	24	30	V
	I_{VDD} = 0A @ V_{VHH} > 8V	2,3	V_{VHH} -V_{VSS}	5.5	7	30	V
Quiescent Current	V_{L+} -V_{L-} = 24V	21, 24	I_{L+}			15	mA
	V_{VHH} -V_{VSS} = 7V	2,3	I_{VHH}			5	mA
Input Voltage	V_I = $V_{C/Q}$ – V_{L-}	22, 24	V_I	-1		34	V
Operating Temperature			ϑ_{AMB}	-40		85	°C

4.2 VOLTAGE REGULATORS, OVERVOLTAGE PROTECTION

Table 4 - Voltage Regulators, Overvoltage Protection

Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
Supply Voltage (Sensor)		21, 24	V_{L+} - V_{L-}	9	24	30	V
Supply Voltage Ripple		21	$V_{L+RIPPLE}$			5	V
Output Voltage VDD	5 V (CCE4501 – 5V)	5, 3	VDD	4.75	5	5.25	V
	3.3 V (CCE4501 – 3.3V)	5, 3	VDD	3.1	3.3	3.5	V
Output Voltage VHH		2, 3	VHH	5.5	7	8.5	V
Switching Frequency DC/DC Converter			f_{SWITCH}	0.8		1.4	MHz
Inductance DC/DC Converter		2, 1	L_{EXT}		33		µH
Ripple VHH	CVHH >= 10 µF ESR < 0.1 Ω @ 100kHz	2	$V_{VHH-RIPPLE}$			100	mV
Voltage Drop LDO		2, 5	V_{VHH}-V_{VDD}	1			V
Output Current VHH	DC/DC converter active	2	I_{VHH}			60	mA
Output Current VDD		5	I_{VDD}			50	mA
Temperature Coefficient VDD		2, 5	TK_{VDD5}			200	ppm/K
Power Supply Rejection Ratio (LDO)	C_{VHH}=100nF, C_{VDD}=4,7uF, f<300kHz		PSRR		46		dB
Voltage Limitation L+	Referred to L-	21	V_{L+LIM}	60		80	V
Output Noise Voltage (LDO)	f=10 Hz ... 500 kHz	5	V_{NOISE}		TBD		V
Load Rejection	I_{VDD} = 1mA switched	3				10	mV

4.3 SWITCHING OUTPUTS CQ_1, CQ_2

Table 5 - Switching Outputs

Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
Voltage CQ_x		22, 23	V_{CQ_MAX}			50	V
Voltage Drop HS/LS Driver	I_{CQ_OUT} = 100mA	22, 23	V_{DROP}			1	V
Permanent Output Current	I_{CQ_OUT}	22, 23				200	mA
Peak Output Current	Maximum duration t_{AK}	22, 23		200		500	mA
Peak Current Duration	thermally limited	22, 23	t_{AK}			1	s
Inductive Load CQ_x		22, 23	L_{LOAD}		10		mH
Inductive Load CQ_x		22, 23	C_{LOAD}		1		µF
Rise Time LS Driver	Capacitive load C_{CQ_EXT} = 20pF	22, 23	$t_{R\_CQ\_LS}$		50		ns
Rise Time HS Driver	Capacitive load C_{CQ_EXT} = 20pF	22, 23	$t_{R\_CQ\_HS}$		50		ns
Fall Time LS Driver	Capacitive load C_{CQ_EXT} = 20pF	22, 23	$t_{F\_CQ\_LS}$		50		ns
Fall Time HS Driver	Capacitive load C_{CQ_EXT} = 20pF	22, 23	$t_{F\_CQ\_HS}$		50		ns
Switch On Time CQ_x	$t_{CQ\_ON} = t_{R\_CQ\_LS} + t_{R\_CQ\_HS} + t_{LH\_BBM}$	22, 23	t_{CQ_ON}	0		1.5	µs
Switch Off Time CQ_x	$t_{CQ\_OFF} = t_{F\_CQ\_LS} + t_{F\_CQ\_HS} + t_{LH\_BBM}$	22, 23	t_{CQ_OFF}	0		1.5	µs
Break before Make Delay	$t_{LH\_BBM} \approx t_{HL\_BBM}$	22, 23	t_{LH_BBM}, t_{HL_BBM}	1		30	ns
Short Circuit Current	±10% Accuracy	22, 23	I_{SHORT}		200		mA
Short Circuit Detection Time	see H/V configuration register	22, 23	t_{KDET}	100		400	µs
Short Circuit Polling Time		22, 23	t_{KPOLL}	100		400	ms
Pull-up/down Resistor	external	22, 23	R_K	15		33	kΩ
Pull-up/down Current Source	alternatively to R_K	22, 23	I_K	0.8	1	1.2	mA

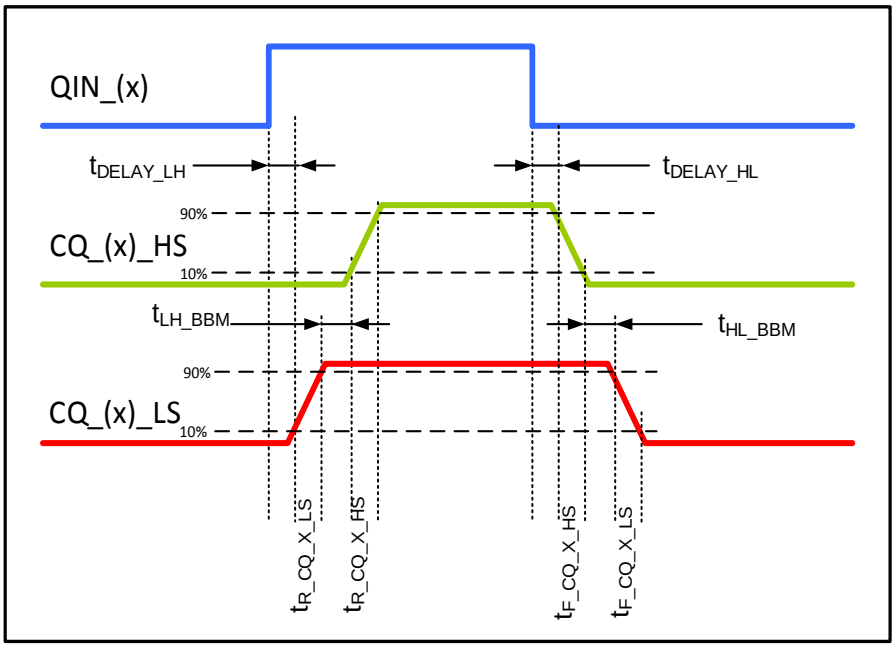


Figure 3 - Timing CQ_x Outputs ("Break before Make")

4.4 DIGITAL INPUTS

Table 6 - Digital Inputs

Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
Input Voltage LOW	V_{DD} - V_{SS} = 3.3 V	8, 9, 11, 13, 14, 15, 17, 18, 19, 20	V_{IN_L}	1		1.6	V
Input Voltage HIGH	V_{DD} - V_{SS} = 3.3 V	8, 9, 11, 13, 14, 15, 17, 18, 19, 20	V_{IN_H}	1.7		2.2	V
Input Voltage LOW	V_{DD} - V_{SS} = 5.0 V	8, 9, 11, 13, 14, 15, 17, 18, 19, 20	V_{IN_L}	1		2	V
Input Voltage HIGH	V_{DD} - V_{SS} = 5.0 V	8, 9, 11, 13, 14, 15, 17, 18, 19, 20	V_{IN_H}	2.8		3.4	V
Input Capacitance		8, 9, 11, 13, 14, 15, 17, 18, 19, 20	C_{IN}			5	pF
Input Leakage Current		8, 9, 11, 13, 14, 15, 17, 18, 19, 20	I_{ILEAK}	-5		5	µA

4.5 DIGITAL OUTPUTS

Table 7 - Digital Outputs

Parameter	Conditions	Pins	Name	Min	Typ	Max	Unit
Output Voltage LOW	V_{DD} - V_{SS} = 3.3 V, 5 V I_{OUT_LOW} = 2 mA	6, 7, 10, 12, 16, 19	V_{OUT_L}			0.5	V
Output Voltage HIGH	V_{DD} - V_{SS} = 3.3 V, 5 V I_{OUT_HIGH} = 2 mA	6, 7, 10, 12, 16, 19	V_{OUT_H}	2.8			V
Output Leakage Current	Tri-state active	6, 7, 10, 12, 16, 19	I_{OLEAK}	-5		5	µA
Output Capacitance		6, 7, 10, 12, 16, 19	C_{OUT}		5		pF

4.6 PROTECTION CIRCUIRY

The CQ_x outputs are protected through the current limiting intrinsic n-well diodes. The supply voltage L+ is protected by an integrated reverse-polarity protection diode.

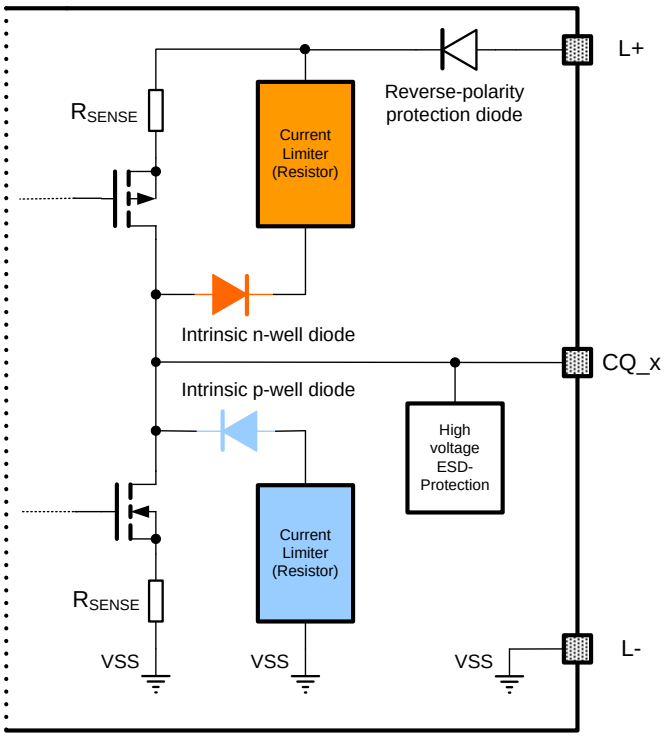


Figure 4 - Reverse-polarity protection senses at CQ_x and L+

5 FUNCTIONAL DESCRIPTION

5.1 OVERALL FUNCTIONAL DESCRIPTION

The IC integrates one IO-Link capable bidirectional switching interface, which can be used as SIO or UART transceiver, and one IO-Link compliant switching output. It includes a hardware IO-Link frame handler based on the UART interface. The CCE4501 can be controlled via IO-Pins or the SPI. The pin CQ_1 is bi directional, pin CQ_2 is an output.

The logic core can be clocked by an external quartz or the integrated RC oscillator. The CLK_EXT pin is used for external clocking. The frequency must be 3.6864 MHz.

5.2 CONFIGURATION BITS K1, K2

Table 8 - Configuration Bits

K1	K2	EXT_CLK	Functional Mode
0	0	Output	Functional Mode using internal RC oscillator (default)
0	1	Input	Functional Mode using external quartz oscillator
1	0	Input	Reserved for testing (programming)
1	1	Input	Reserved for testing (scantest)

5.3 REGISTER DESCRIPTION

5.3.1 Register Definitions

Table 9 - Register Definitions

Address	Name	Description	Access
0x00-0x59	-	reserved	-
0x60	CFG	IC Configuration	Read/Write
0x61	HV_CTRL	H/V Output Control	Read/Write
0x62	UART	UART Data Register	Read/Write
0x63	HV_CFG	H/V Output Configuration	Read/Write
0x64-0x71	-	reserved	-
0x72	MPLD	Master PD Length	Read/Write
0x73	DPDL	Device PD Length	Read/Write
0x74	FH_OUT	Frame Handler Output	Write
0x75	FH_IN	Frame Handler Input	Read
0x75-0x7E	-	reserved	-
0x7F	FH_RST	Frame Handler Reset	Write
0x80-0xFF	-	reserved	-

5.3.2 CFG (0x60)

The IC Configuration register controls the behavior of the circuit. It is possible to configure the SPI mode, the communication speed used by the integrated UART and the frame handler mode.

Table 10 - CFG

Bit	7	6	5	4	3	2	1	0
Name	FH	-	-	-	UART		SPI	
Default	0				0		0	

SPI *SPI-Mode*

0h: SIO Mode (default)
1h: UART Mode
2h: IO-Link Mode
3h: reserved

UART *UART Baudrate*

0h: UART disabled (default)
1h: COM1 (4.8 kBit/s)
2h: COM2 (38.4 kBit/s)
3h: COM3 (230.4 kBit/s)

FH *Frame Handler Mode*

0h: Device Modus
1h: Master Modus

5.3.3 HV_CTRL (0x61)

The H/V Output Setup register controls the switching outputs CQ_1 and CQ_2.

Table 11 - HV_CTRL

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	EN1	-	OUT1	OUT2
Default					0		0	0

OUT1 *Channel 1 Driver Output Value*
OUT2 *Channel 2 Driver Output Value*
EN1 *Channel 1 Driver Output Enable*

If the SIO mode is active, both channels can be controlled by the logically OR-ed inputs QIN_1, QENX_1 and QIN_2 and their corresponding control bits of this register. Changes will have no effect on Channel 1 if the IC is in UART or IO-Link Mode.

5.3.4 UART (0x62)

If the channel is configured in UART mode, reading this register returns a received UART character. Writing to this register sends the given character using the integrated UART.

Table 12 - UART

Bit	7	6	5	4	3	2	1	0
Name	DATA (UART_TX write / UART_RX read)							
Default	00h							

DATA *UART character*

5.3.5 HV_CFG (0x63)

This register is used to setup the driver mode and short detection behavior. The default values are programmable using OTP cells.

Table 13 - HV_CFG

Bit	7	6	5	4	3	2	1	0
Name	SDM2		CHM2		SDM1		CHM1	
Default	SDM1		CHM1		programmable		programmable	

CHM1/CHM2 *Channel 1/2 Driver Configuration*

0h: Channel disabled
1h: N-Mode
2h: P-Mode
3h: Push-Pull

SDM1/SDM2 *Channel 1/2 Short Detection Behavior*

0h: Polling disabled
1h: t_{KDET}=100µs / t_{KPOLL}=100ms
2h: t_{KDET}=200µs / t_{KPOLL}=200ms
3h: t_{KDET}=400µs / t_{KPOLL}=400ms

The short circuit indicator signal SDX_x is low if a short gets detected and the corresponding channel will be deactivated. After detection of a short-circuit the persistence will be periodically (t=t_{KPOLL}) checked by activating the channel for a short time (t<=t_{KDET}).

It is possible to disable the automatic deactivation of the channel. However a high current will be detected and indicated. Note that high current flow over a longer period of time may cause damage to the IC.

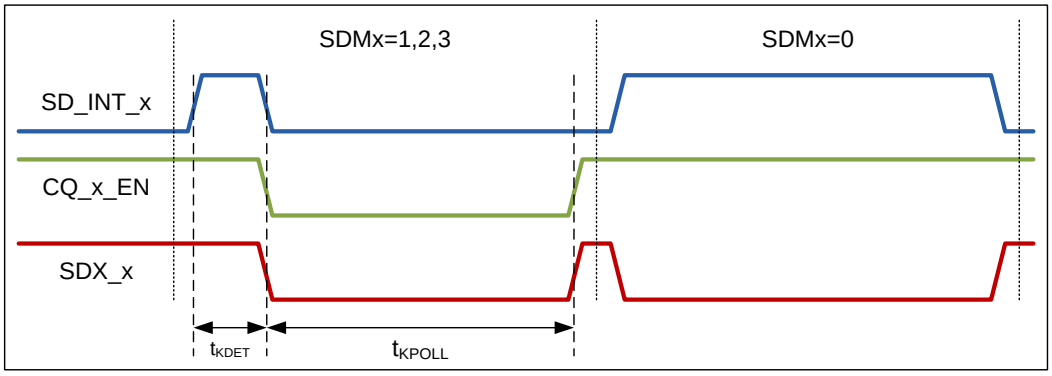


Figure 5 - Short Detection Behavior

5.3.6 MPDL (0x72)

This register configures the length of the master process data in bytes. Valid values are 0-2.

Table 14 - MPDL

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	MAS_LEN	
Default							0h	

MAS_LEN *Master Process Data Length*

0x0: 0 Byte
0x1: 1 Byte
0x2: 2 Byte
0x3: reserved

5.3.7 DPDL (0x73)

This register configures the length of the device process data in bytes. Valid values are 0-2.

Table 15 - DPDL

Bit	7	6	5	4	3	2	1	0
Name	-	-	-	-	-	-	DEV_LEN	
Default							0h	

DEV_LEN *Device Process Data Length*

0x0: 0 Byte
0x1: 1 Byte
0x2: 2 Byte
0x3: reserved

5.3.8 FH_OUT (0x74)

Writing to this register buffers the given characters for an outgoing message, which gets sent over the integrated UART.

Table 16 - FH_OUT

Bit	7	6	5	4	3	2	1	0
Name	TRANS_DAT							
Default	-							

5.3.9 FH_IN (0x75)

Reading this register returns the buffered UART characters of a received IO-Link message.

Table 17 - FH_IN

Bit	7	6	5	4	3	2	1	0
Name	RECV_DAT							
Default	0h							

5.3.10 FH_RST (0x7F)

This is a dummy register. The integrated frame handler will be reset after a write access to it.

5.4 SPI (SERIAL PERIPHERAL INTERFACE)

5.4.1 Signal Description

Table 18 - Signal Description

Name	Type	Description
MOSI	Input	Data input
MISO	Output	Data output
SCLK	Input	Clock input (f_{MAX} = 20 MHz)
SSX	Input	Slave select (active-low)
INTX	Output	Interrupt output for microcontroller (active-low)

5.4.2 Data Format

The CCE4501 is configured as SPI slave and uses the CPOL=0, CPHA=0 configuration. During each transaction, a number of 2 bytes will be transferred.

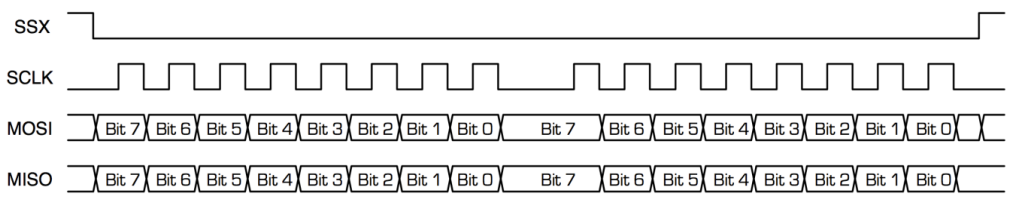


Figure 6 - Timing Diagram

5.4.3 MOSI Format

Table 19 - MOSI Format

Bit	7	6	5	4	3	2	1	0
1st Byte	ADR[6:0]							R/W
2nd Byte	DATA[7:0]							

1st Byte *SPI Control Byte*

ADR[6:0] register address

R/W defines if register access is read (0b1) or write (0b0)

2nd Byte *Input Data Byte*

DATA[7:0] value which gets written into the defined register on write access; ignored on read access

5.4.4 MISO Format

Table 20 - MISO Format

Bit	7	6	5	4	3	2	1	0
1st Byte	STAT[7:0]							
2nd Byte	DATA[7:0]							

1st Byte *SPI Status Byte*

STAT[7:0] status of the IC (see 5.4.5)

2nd Byte *Output Data Byte*

DATA[7:0] current value of the accessed register

5.4.5 STAT Format

The IC uses the SPI status byte to indicate its current status. Depending on the mode, which is set in the configuration register, STAT changes its format.

Table 21 - STAT Format

Mode	Mode Name	7	6	5	4	3	2	1	0
0b00	SIO Mode	TEMP	-	-	-	SD1	SD2	HL1	WURQ
0b01	UART Mode	TEMP	RX_ERR	RX_RDY	TX_RDY	SD1	SD2	-	-
0b10	IO-Link Mode	TEMP	FH_STAT			SD1	SD2	-	TOUT

TEMP *High temperature indicator*

RX_ERR *UART parity error*

RX_RDY *UART receiver ready (input available)*

TX_RDY *UART transmitter ready*

FH_STAT	*Frame handler state* 0: idle 1: reserved 2: transmission active 3: transmission active; further output required 4: receiving active 5: receiving active; new input available 6: receiving done; message valid 7: receiving done; checksum error
SD1/SD2	*Short Detection*
HL1	*CQ_1Input*
WURQ	*Wake-Up detected*
TOUT	*Frame handler timeout (after 25 T_{BIT})*

5.4.6 Interrupt INTX

An interrupt is always triggered, as soon as one of the SPI status bits has changed.

5.5 IO-LINK FRAME HANDLER

The integrated frame handler is fully compliant to the current IO-Link specification version 1.1. Frame types 0, 1.1-1.2 and 2.1-2.6 are supported. An automatic checksum calculation and verification is integrated. The frame timing is monitored.

If an error or a timeout occurs during frame processing, the frame handler needs to be reset by a write access to the FH_RST register.

5.5.1 Device Mode

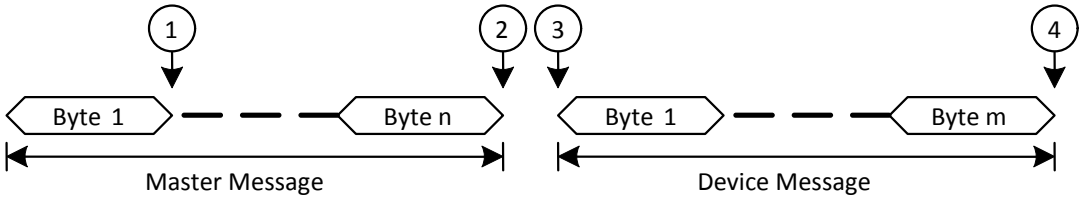


Figure 7 - Device Mode Handling

1. Until the first byte of the master message is received, the frame handler is in idle state. Then it changes to receive state and displays each byte by its state (FH_STAT) and by setting an interrupt. The user can read out the data using the FH input register.
2. When the last byte of the master message is detected, the checksum verification will be communicated via the appropriate status. The frame handler changes into transmit state and waits for data from device protocol.
3. Once the first byte of the device protocol was written into the FH output register, the transmission process is started. The checksum in the *m* byte is generated automatically.
4. While sending the last byte the frame handler is reset and goes back into idle state.

5.5.2 Master-Mode

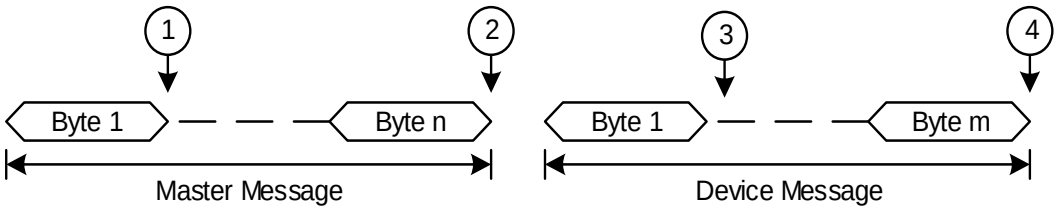


Figure 8 - Master Mode Handling

1. Until the first byte of master message is written into the buffer by the user, the frame handler stays in idle state. It changes into transmit state after all bytes of the message are stored and sends the message. The checksum in Byte 2 is generated automatically.
2. When the last byte of the master message was sent, the frame handler changes into receive state.
3. Each received byte is indicated by an interrupt. The user can read out the data using the FH input register.
4. When the last byte gets read out by the user, the checksum verification will be communicated via the appropriate status. The frame handler is reset and goes back into idle state.

6 APPLICATION NOTES

6.1 APPLICATION WITH ACTIVE DC/DC CONVERTER

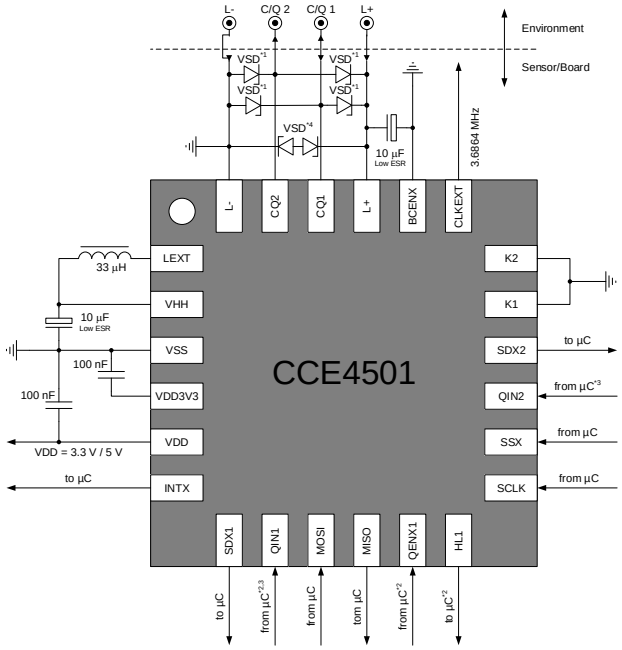


Figure 9 - Application with active DC/DC Converter

6.2 APPLICATION WITHOUT ACTIVE DC/DC CONVERTER

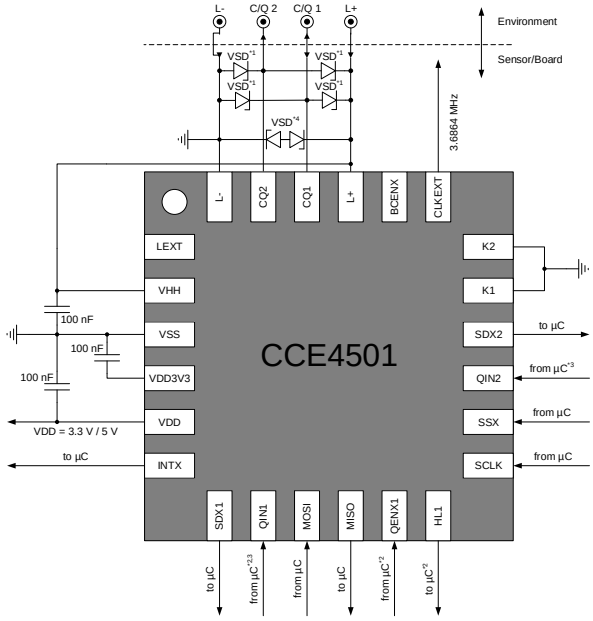


Figure 10 - Application without active DC/DC Converter

*1) uni-directional TVS diode such as SMAJ33A
*2) This micro controller port is only used in SIO mode
*3) Tie signal to ground if chip is used as transceiver controlled over SPI
*4) bi-directional TVS diode such as SMAJ33A

7 PACKAGE OUTLINE

7.1 QFN24 PACKAGE

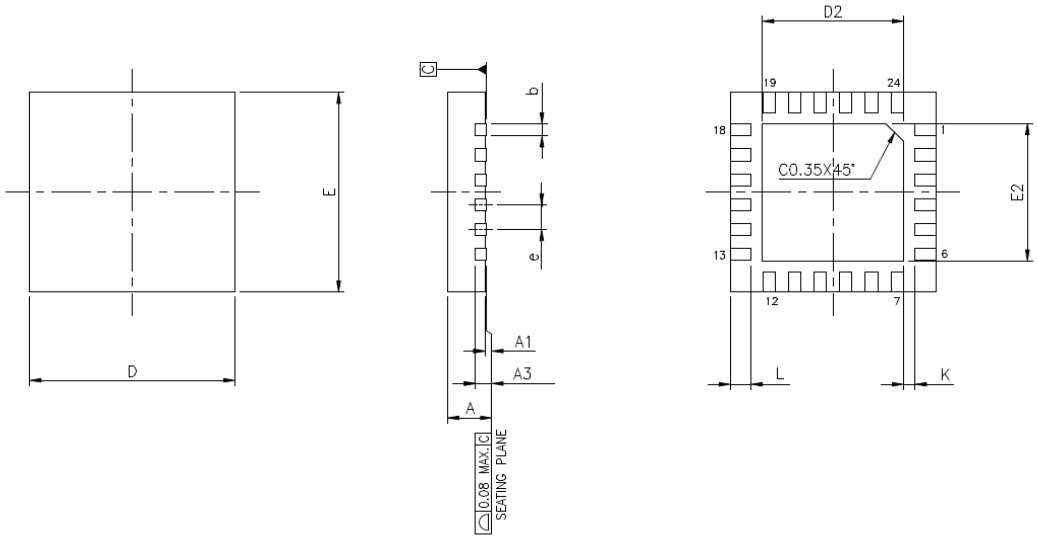


Figure 11 - QFN24 Package

Symbol	A	A1	A3	b	D	E	e	L	K	D2	E2
Min	0.70	0.00	0.20 REF.	0.18	4.00 BSC.	4.00 BSC.	0.50 BSC.	0.35	0.20	2.50	2.50
Typ	0.75	0.02		0.25				0.40	-	2.60	2.60
Max	0.80	0.05		0.30				0.45	-	2.65	2.65

UNIT : mm

NOTES :

1. JEDEC OUTLINE : MO-220 WGGD-6.
2. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.15mm AND 0.30mm FROM THE TERMINAL TIP. IF THE TERMINAL HAS THE OPTIONAL RADIUS ON THE OTHER END OF THE TERMINAL, THE DIMENSION b SHOULD NOT BE MEASURED IN THAT RADIUS AREA.
3. THE MINIMUM "K" VALUE OF 0.20mm APPLIES.
4. BILATERAL COPLANARITY ZONE APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.

8 TAPE AND REEL INFORMATION

8.1 TAPE QFN24 PACKAGE

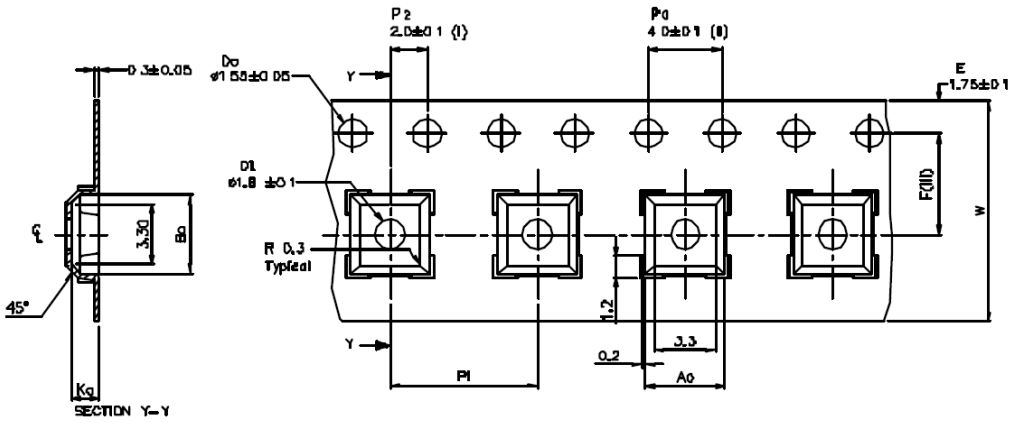


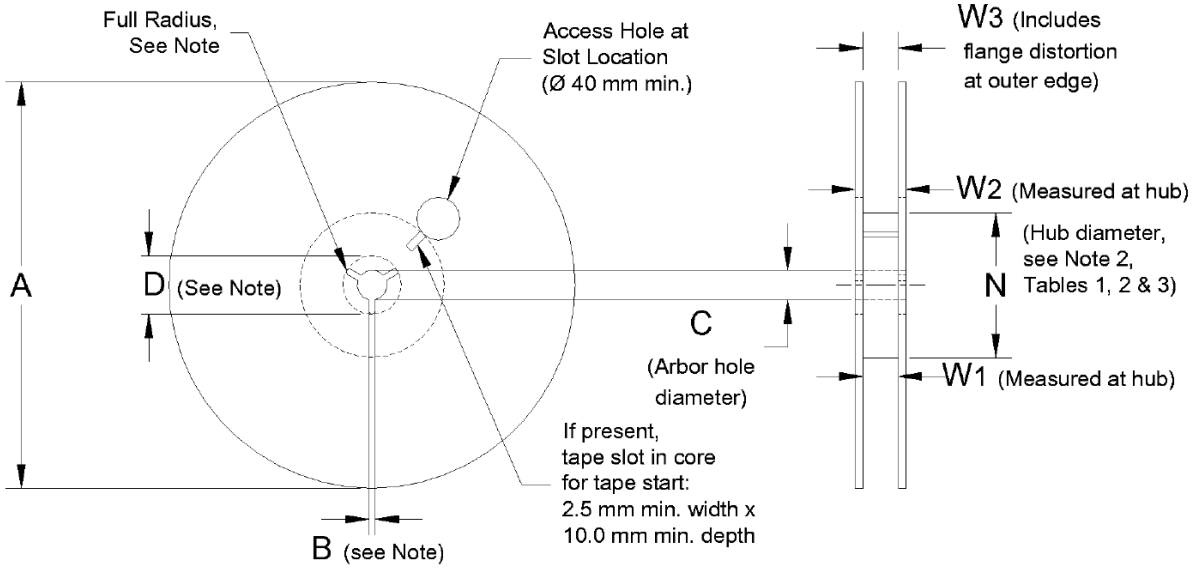
Figure 12 - Tape Dimensions

Ao	4.30 +/– 0.1
Bo	4.30 +/– 0.1
Ko	1.50 +/– 0.1
F	5.50 +/– 0.1
P1	8.00 +/– 0.1
W	12.00 +/– 0.3

(I) Measured from centreline of sprocket hole to centreline of pocket.
(II) Cumulative tolerance of 10 sprocket holes is ± 0.20
(III) Measured from centreline of sprocket hole to centreline of pocket.
(IV) Other material available.

ALL DIMENSIONS IN MILLIMETRES UNLESS OTHERWISE STATED

8.2 REEL INFORMATION



Note: Drive spokes optional; if used, dimensions B and D shall apply.

Figure 13 - Reel Dimensions

Symbol	A	B	C	D	W_1 QFN24
Min	-	1.5	12.8	20.2	13.25
Typ	-	-	13.0	-	-
Max	330	-	13.5	-	13.75

9 ORDERING INFORMATION

Parts can be ordered as 5V or 3.3V output voltage VDD option. Please take the corresponding order no. from the table and contact info@creativechips.com for an individual quote.

Part	Order No.	VDD Option	Delivery	Quantity
CCE4501	CCE4501 – 5V	5V	Tape & Reel	4.000
CCE4501	CCE4501 – 3.3V	3.3V	Tape & Reel	4.000

10 REVISION HISTORY

Revision	Date	Author	Description
1.0	19.04.2011	jw	First version
1.1	26.07.2011	jw	Pull up QENX_1, changed applications & drivers
1.2	05.12.2011	AS/jw	General revision
1.3	16.04.2012	jw	Application Notes updated
1.4	30.04.2012	jw	Corrected Application Notes, removed SSOP24 package
1.5	22.06.2015	Kw	Updated formats

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