Version: 3.0

TECHNICAL SPECIFICATION

MODEL NO: ED029TC1

The content of this information is subject to be changed without notice.
Please contact E Ink or its agent for further information.

☐Customer's Confirmation

Customer _____

Date _____

By _____

☐E Ink's Confirmation

Approve By Sean Chen

Confirmed By Freemen Chuang

Prepared By Joe Li

Revision History

Rev.	Issued Date	Revised Contents
1.0	April 14, 2016	New
2.0	June 3, 2016	Add border dimension in the drawing
3.0	Oct. 12, 2016	Revise FPC pin sequence in the drawing at page 5 Revise connector type at page 6

TECHNICAL SPECIFICATION

CONTENTS

1. General Description

ED029TC1 is a reflective electrophoretic E Ink® technology display module based on active matrix TFT substrate. It has 2.9" active area with 296×128 pixels, the display is capable to display images at 1-bit white and black full display capabilities. An integrated circuit contains gate buffer, source buffer, interface, timing control logic, oscillator, DC-DC, SRAM, LUT, VCOM, and border are supplied with each panel.

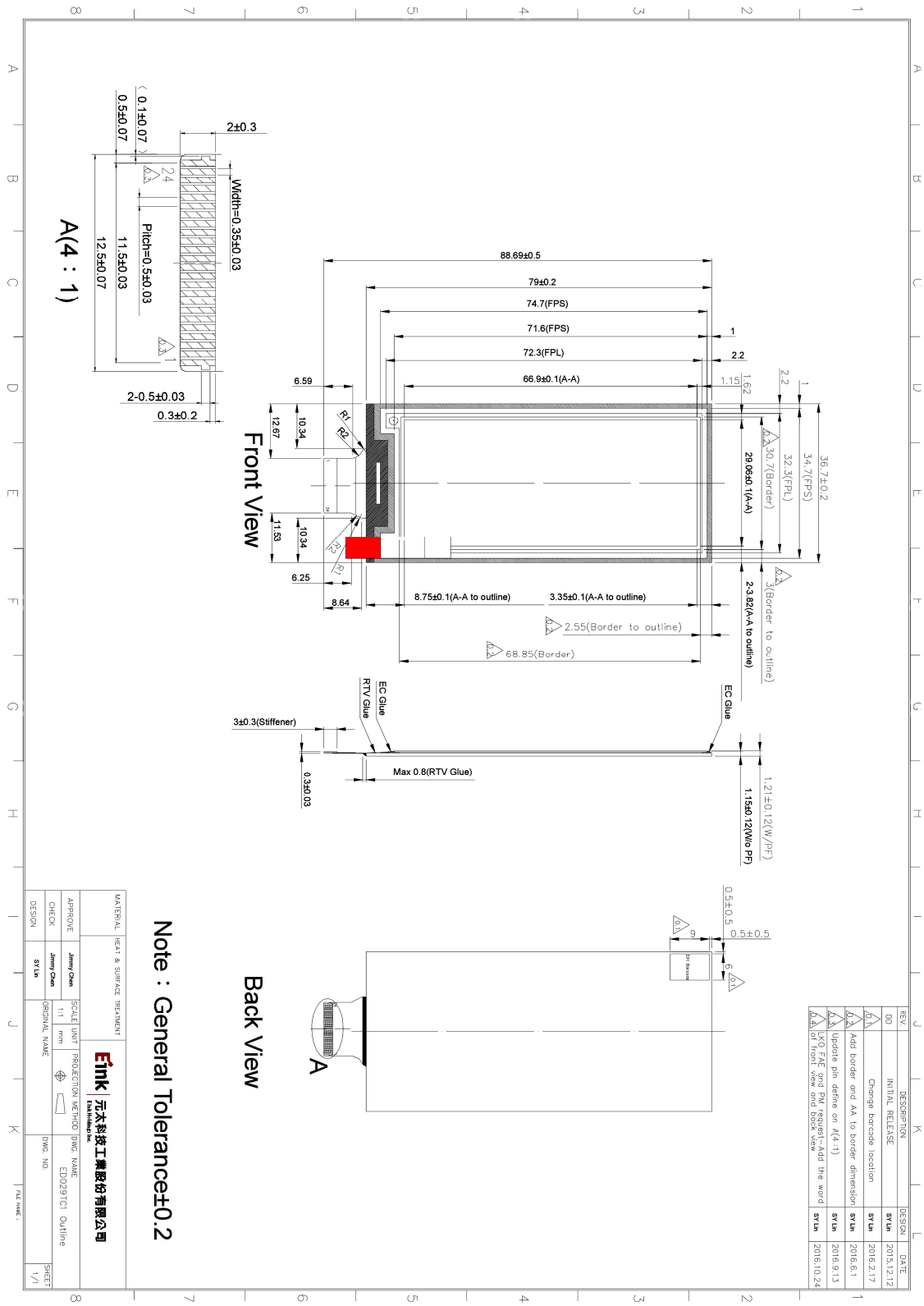
2. Features

- High contrast
- High reflectance
- Ultra wide viewing angle
- Ultra low power consumption
- Pure reflective mode
- Bi-stable
- Commercial temperature range
- Landscape, portrait mode
- Antiglare hard-coated front-surface
- Low current deep sleep mode
- On chip display RAM
- Waveform stored in On-chip OTP
- Serial peripheral interface available
- On-chip oscillator
- On-chip booster and regulator control for generating VCOM, Gate and source driving voltage
- I2C Signal Master Interface to read external temperature sensor
- Available in COG package IC thickness 280um

3. Mechanical Specifications

Parameter	Specifications	Unit	Remark
Screen Size	2.9	Inch	
Display Resolution	296(H)×128(V)	Pixel	Dpi: 112
Active Area	66.9(H)×29.06(V)	mm	
Pixel Pitch	0.227×0.226	mm	
Pixel Configuration	Square		
Outline Dimension	79.0(H)×36.7(V) ×1.15(D)	mm	without masking film
Weight	4±0.5	g	

4. Mechanical Drawing of Display Module



5. Input/Output Interface

5-1) Connector type: AYF532435

Pin Assignment

Pin Assignment			
Pin #	**Type**	**Single**	**Description**
1		NC	No connection and do not connect with other NC pins
2	O	GDR	N-Channel MOSFET Gate Drive Control
3	O	RESE	Current Sense Input for the Control Loop
4		NC	No connection and do not connect with other NC pins
5	P	VDHR	Positive source driver voltage for Red (+2.4V ~ +11V)
6	O	TSCL	I2C Interface to digital temperature sensor Clock pin
7	I/O	TSDA	I2C Interface to digital temperature sensor Date pin
8	I	BS	Bus selection pin; L: 4-wire IF. **H: 3-wire IF. (Default)**
9	O	BUSY_N	Busy state output pin
10	I	RST_N	Reset
11	I	DC	Data /Command control pin
12	I	CSB	Chip Select input pin
13	O	SCL	serial clock pin (SPI)
14	I/O	SDA	serial data pin (SPI)
15	P	VDD	Supply voltage
16	P	VDD	Supply voltage
17	P	GND	Ground
18	P	VDDDO	Core logic power pin
19		NC	No connection and do not connect with other NC pins
20	P	VSH	Positive Source driving voltage
21	P	VGH	Positive Gate driving voltage
22	P	VSL	Negative Source driving voltage
23	P	VGL	Negative Gate driving voltage
24	P	VCOM	VCOM driving voltage

Note 5-1: This pin (CS#) is the chip select input connecting to the MCU. The chip is enabled for MCU communication only when CS# is pulled Low.

Note 5-2: This pin (D/C#) is Data/Command control pin connecting to the MCU. When the pin is pulled HIGH, the data will be interpreted as data. When the pin is pulled Low, the data will be interpreted as command.

Note 5-3: This pin (RES#) is reset signal input. The Reset is active Low.

Note 5-4: This pin (BUSY) is Busy state output pin. When Busy is low, the operation of chip should not be interrupted and any commands should not be issued to the module. The driver IC will put Busy pin low when the driver IC is working such as:

- Outputting display waveform; or
- Programming with OTP
- Communicating with digital temperature sensor

Note 5-5: This pin (BS1) is for 3-line SPI or 4-line SPI selection. When it is “Low”, 4-line SPI is selected. When it is “High”, 3-line SPI (9 bits SPI) is selected. Please refer to below Table.

Table: Bus interface selection

BS1	MPU Interface
L	4-lines serial peripheral interface (SPI)
H	3-lines serial peripheral interface (SPI) – 9 bits SPI

6. Command Table

W/R: 0: Write cycle 1: Read cycle C/D: 0: Command 1: Data D7~D0: -: Don't care #: Valid Data

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
1	Panel Setting (PSR)	0	0	0	0	0	0	0	0	0	0		00h
		0	1	#	#	#	#	#	#	#	#	RES[1:0],REG,KW/R,UD, SHL,SHD_N,RST_N	0Fh
2	Power Setting (PWR)	0	0	0	0	0	0	0	0	0	1		01h
		0	1	-	-	-	-	-	-	#	#	VDS_EN,VDG_EN	03h
		0	1	-	-	-	-	-	#	#	#	VCOM_HV,VGHL_LV[1:0]	00h
		0	1	-	-	#	#	#	#	#	#	VDH[5:0]	26h
		0	1	-	-	#	#	#	#	#	#	VDL[5:0]	26h
		0	1	-	-	#	#	#	#	#	#	VDHR[5:0]	03h
3	Power OFF(POF)	0	0	0	0	0	0	0	0	1	0		02h
4	Power OFF Sequence Setting(PFS)	0	0	0	0	0	0	0	0	1	1		03h
		0	1	-	-	#	#	-	-	-	-	T_VDS_OF	00h
5	Power ON(PON)	0	0	0	0	0	0	0	1	0	0		04h
6	Power ON Measure(PMES)	0	0	0	0	0	0	0	1	0	1		05h
7	Booster Soft Start(BTST)	0	0	0	0	0	0	0	1	1	0		06h
		0	1	#	#	#	#	#	#	#	#	BT_PHA[7:0]	17h
		0	1	#	#	#	#	#	#	#	#	BT_PHB[7:0]	17h
		0	1	-	-	#	#	#	#	#	#	BT_PHC[5:0]	17h
8	Deep Sleep	0	0	0	0	0	0	0	1	1	1		07h
		0	1	1	0	1	0	0	1	0	1	Check code	A5h
9	Display Start Transmission 1(DTM1, white/black Data) (x-byte command)	0	0	0	0	0	1	0	0	0	0	B/W Pixel Data (160x296)	10h
		0	1	#	#	#	#	#	#	#	#	KPXL[1:8]	00h
		0	1	..	..	..	..	..	..	..	..	..	…
		0	1	#	#	#	#	#	#	#	#	KPXL[n-1:n]	00h
10	Data Stop	0	0	0	0	0	1	0	0	0	1		11h
		1	1	#	-	-	-	-	-	-	-		00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
11	Display Refresh(DRF)	0	0	0	0	0	1	0	0	1	0		12h
12	Display Start Transmission 2(DTM2, Red Data) (x-byte command)	0	0	0	0	0	1	0	0	1	1	B/W Pixel Data (160x296)	13h
		0	1	#	#	#	#	#	#	#	#	RPXL[1:8]	00h
		0	1	..	..	..	..	..	..	..	..	..	…
		0	1	#	#	#	#	#	#	#	#	RPXL[n-1:n]	00h
13	VCOM LUT(LUTC) (45-byte command, structure of bytes 2~7 repeated)	0	0	0	0	1	0	0	0	0	0		20h
14	W2W LUT (LUTWW) (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	0	1		21h
15	B2W LUT (LUTBW / LUTR) (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	1	0		22h
16	W2B LUT (LUTWB / LUTW) (43-byte command, structure of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	0	1	1		23h
17	B2B LUT (LUTBB / LUTB) (43-byte command, sturcture of bytes 2~7 repeated 7 times)	0	0	0	0	1	0	0	1	0	0		24h
18	PLL control(PLL)	0	0	0	0	1	1	0	0	0	0		30h
		0	1	-	-	#	#	#	#	#	#	M[2:0],N[2:0]	3Ch
19	Temperature Sensor Calibration (TSC)	0	0	0	1	0	0	0	0	0	0		40h
		1	1	#	#	#	#	#	#	#	#	LM[10:3]/TSR[7:0]	00h
		1	1	#	#	#	-	-	-	-	-	LM[2:0]/-	00h
20	Temperature Sensor Selection (TSE)	0	0	0	1	0	0	0	0	0	1		41h
		0	1	#	-	-	-	#	#	#	#	TSE,TO[3:0]	00h
21	Temperature Sensor Write(TSW)	0	0	0	1	0	0	0	0	1	0		42h
		0	1	#	#	#	#	#	#	#	#	WATTR[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WMSB[7:0]	00h
		0	1	#	#	#	#	#	#	#	#	WLSB[7:0]	00h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
22	Temperature Sensor Read (TSR)	0	0	0	1	0	0	0	0	1	1		43h
		1	1	#	#	#	#	#	#	#	#	RMSB[7:0]	00h
		1	1	#	#	#	#	#	#	#	#	RLSB[7:0]	00h
23	Vcom and data interval setting (CDI)	0	0	0	1	0	1	0	0	0	0		50h
		0	1	#	#	#	#	#	#	#	#	VBD[1:0],DDX[1:0],CDI[3:0]	D7h
24	Lower Power Detection (LPD)	0	0	0	1	0	1	0	0	0	1		51h
		1	1	-	-	-	-	-	-	-	#	LPD	01h
25	TCON setting (TCON)	0	0	0	1	1	0	0	0	0	0		60h
		0	1	#	#	#	#	#	#	#	#	S2G[3:0],G2S[3:0]	22h
26	Resolution setting (TRES)	0	0	0	1	1	0	0	0	0	1		61h
		0	1	#	#	#	#	#	0	0	0	HRES[7:3]	00h
		0	1	-	-	-	-	-	-	-	#	VRES[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
27	Revision(REV)	0	0	0	1	1	1	0	0	0	0		70h
		0	1	#	#	#	#	#	#	#	#	LUT_REV[7:0]	00h
28	Get Status (FLG)	0	0	0	1	1	1	0	0	0	1		71h
		1	1	-	#	#	#	#	#	#	#	PTL_FLAG,I^{2}C_BUSY,DATA_FLAG,PON,POF,BUSY	02h
29	Auto Measurement Vcom	0	0	1	0	0	0	0	0	0	0		80h
		0	1	-	-	#	#	#	#	#	#	AMVT[1:0], XON,AMVS, AMV,AMVE	10h
30	Read Vcom Value(VV)	0	0	1	0	0	0	0	0	0	1		81h
		1	1	-	-	#	#	#	#	#	#	VV[5:0]	00h
31	VCM_DC Setting (VDCS)	0	0	1	0	0	0	0	0	1	0		82h
		0	1	-	-	#	#	#	#	#	#	VDCS[5:0]	00h
32	Partial Window (PTL)	0	0	1	0	0	1	0	0	0	0		90h
		0	1	#	#	#	#	#	0	0	0	HRST[7:3]	00h
		0	1	#	#	#	#	#	1	1	1	HRED[7:3]	07h
		0	1	-	-	-	-	-	-	-	#	VRST[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	-	-	-	-	-	-	-	#	VRED[8:0]	00h
		0	1	#	#	#	#	#	#	#	#		00h
		0	1	-	-	-	-	-	-	-	#	PT_SCAN	01h

#	Command	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0	Registers	Default
33	Partial In (PTIN)	0	0	1	0	0	1	0	0	0	1		91h
34	Partial Out (PTOUT)	0	0	1	0	0	1	0	0	1	0		92h
35	Power Saving (PWS)	0	0	1	1	1	0	0	0	1	1		E3h
		0	1	#	#	#	#	#	#	#	#	VCOM_W[3:0],SD_W[3:0]	00h

(1) Panel Setting (PSR) (Register: R00H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting the panel	0	0	0	0	0	0	0	0	0	0
	0	1	RES 1	RES 0	REG_EN	BWR	UD	SHL	SHD_N	RST_N

RES[1:0]: Display Resolution setting (source x gate)

00b: 96x230 (Default) Active source channels: S0 ~ S95. Active gate channels: G0 ~ G229.

01b: 96x252 Active source channels: S0 ~ S95. Active gate channels: G0 ~ G251.

10b: 128x296 Active source channels: S0 ~ S127. Active gate channels: G0 ~ G295.

11b: 160x296 Active source channels: S0 ~ S159. Active gate channels: G0 ~ G295.

REG_EN: LUT selection

0: LUT from OTP. (Default)

1: LUT from register.

BWR: Black / White / Red

0: Pixel with B/W/Red. (Default)

1: Pixel with B/W.

UD: Gate Scan Direction

0: Scan down. First line to last line: Gn-1 → Gn-2 → Gn-3 → … → G0

1: Scan up. (default) First line to last line: G0 → G1 → G2 → … → Gn-1

SHL: Source Shift direction

0: Shift left First data to last data: Sn-1 → Sn-2 → Sn-3 → … → S0

1: Shift right. (default) First data to last data: S0 → S1 → S2 → … → Sn-1

SHD_N: Booster Switch

0: Booster OFF, register data are kept, and SEG/BG/VCOM are kept 0V or floating.

1: Booster ON (Default)

When SHD_N become LOW, charge pump will be turned OFF, register and SRAM data will keep until VDD OFF, and SD output and VCOM will remain previous condition. SHD_N may have two conditions: 0v or floating.

RST_N: Soft Reset

1: No effect (Default). Booster OFF, Register data are set to their default values, and SEG/BG/VCOM: 0V

When RST_N become LOW, the driver will be reset, all registers will be reset to their default value. All driver functions will be disabled. SD output and VCOM will base on previous condition. It may have two conditions: 0v or floating.

(2) Power Setting (PWR) (R01H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Selecting Internal/External Power	0	0	0	0	0	0	0	0	0	1
	0	1	-	-	-	-	-	-	VDS_EN	VDG_EN
	0	1	-	-	-	-	-	VCOM_HV	VGHL_LV[1:0]	
	0	1	-	-	VDH[5:0]					
	0	1	-	-	VDL[5:0]					
	0	1	-	-	VDHR[5:0]					

VDS_EN: Source power selection

0: External source power from VDH/VDL pins

1: Internal DC/DC function for generating VDH/VDL

VDG_EN: Gate power selection

0: External gate power from VGH/VGL pins

1: Internal DC/DC function for generating VGH/VGL

VCOM_HV: VCOM Voltage Level

0: VCOMH=VDH+VCOMDC, VCOML=VHL+VCOMDC

1: VCOML=VGH, VCOML=VGL

VGHL_LV[1:0]: VGH / VGL Voltage Level selection.

VGHL_LV	VGHL voltage level
00(Default)	VGH=16V,VGL= -16V
01	VGH=15V,VGL= -15V
10	VGH=14V,VGL= -14V
11	VGH=13V,VGL= -13V

VDH[5:0]: Internal VDH power selection for B/W pixel.(Default value: 100110b)

VDH	VDH_V	VDH	VDH_V
000000	2.4V	…	…
000001	2.6V	100110	10.0V
000010	2.8V	100111	10.2V
000011	3.0V	101000	10.4V
000100	3.2V	101001	10.6V
000101	3.4V	101010	10.8V
000110	3.6V	101011	11.0V
000111	3.8V	(others)	11.0V

VDL[5:0]: Internal VDL power selection for B/W pixel. (Default value: 100110b)

VDL	VDL_V	VDL	VDL_V
000000	-2.4V	…	…
000001	-2.6V	100110	-10.0V
000010	-2.8V	100111	-10.2V
000011	-3.0V	101000	-10.4V
000100	-3.2V	101001	-10.6V
000101	-3.4V	101010	-10.8V
000110	-3.6V	101011	-11.0V
000111	-3.8V	(others)	-11.0V

VDHR[5:0]: Internal VDHR power selection for Red pixel. (Default value: 000011b)

VDHR	VDHR _V	VDHR	VDHR _V
000000	2.4V	…	…
000001	2.6V	100110	10.0V
000010	2.8V	100111	10.2V
000011	3.0V	101000	10.4V
000100	3.2V	101001	10.6V
000101	3.4V	101010	10.8V
000110	3.6V	101011	11.0V
000111	3.8V	(others)	11.0V

(3) Power OFF (POF) (R02H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning OFF the power	0	0	0	0	0	0	0	0	1	0

After the Power Off command, the driver will power off following the Power Off Sequence. This command will turn off charge pump, T-con, source driver, gate driver, VCOM, and temperature sensor, but register data will be kept until VDD becomes OFF. Source Driver output and Vcom will remain as previous condition, which may have 2 condition: 0V or floating.

(4) Power off sequence setting (PFS) (R03H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Setting Power OFF sequence	0	0	0	0	0	0	0	0	1	1
	0	1	-	-	T_VDS_OFF[1:0]		-	-	-	-

T_VDS_OFF[1:0]: Power OFF Sequence of VDH and VDL.

00b: 1frame (Default) 01b: 2 frames 10b: 3frames 11b:4 frame

(5) Power ON (PON) (R04H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Turning ON the Power	0	0	0	0	0	0	0	1	0	0

After the Power ON command, the driver will be powered ON following the Power ON Sequence. Refer to the Power ON Sequence section. In the sequence, temperature sensor will be activated for one time sensing before enabling booster.

(6) Power ON Measure (PMES) (R05H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	1	0	1

This command enables the internal bandgap, which will be cleared by the next POF.

(7) Booster Soft Start (BTST) (R06H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	0	0	0	0	0	1	1	0
Starting data	0	1	BT_PHA7	BT_PHA6	BT_PHA5	BT_PHA4	BT_PHA3	BT_PHA2	BT_PHA1	BT_PHA0
transmission	0	1	BT_PHB7	BT_PHB6	BT_PHB5	BT_PHB4	BT_PHB3	BT_PHB2	BT_PHB1	BT_PHB0
	0	1	-	-	BT_PHC5	BT_PHC4	BT_PHC3	BT_PHC2	BT_PHC1	BT_PHC0

BTPHA[7:6]: Soft start period of phase A.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHA[5:3]: Driving strength of phase A

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4

100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHA[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS

100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHB[7:6]: Soft start period of phase B.

00b: 10mS 01b: 20mS 10b: 30mS 11b: 40mS

BTPHB[5:3]: Driving strength of phase B

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4

100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHB[2:0]: Minimum OFF time setting of GDR in phase B

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS

100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

BTPHC[5:3]: Driving strength of phase C

000b: strength 1 001b: strength 2 **010b: strength 3** 011b: strength 4

100b: strength 5 101b: strength 6 110b: strength 7 111b: strength 8 (strongest)

BTPHC[2:0]: Minimum OFF time setting of GDR in phase C

000b: 0.27uS 001b: 0.34uS 010b: 0.40uS 011b: 0.54uS

100b: 0.80uS 101b: 1.54uS 110b: 3.34uS **111b: 6.58uS**

(8) Deep Sleep (DSLP) (R07H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Deep Sleep	0	0	0	0	0	0	0	1	1	1
	0	1	1	0	1	0	0	1	0	1

After this command is transmitted, the chip would enter the deep-sleep mode to save power.

The deep sleep mode would return to standby by hardware reset.

The only one parameter is a check code, the command would be executed if check code = 0xA5.

(9) Data Start Transmission 1 (DTM1) (R10H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	0	0
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	..	..	..	..	..	..	..	..
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

This command starts transmitting data and writes them into SRAM. To complete data transmission, command DSP (Data transmission Stop) must be issued. Then the chip will start to send data/VCOM for panel.

In B/W mode, this command writes “OLD” data to SRAM.

In B/W/Red mode, this command writes “B/W” data to SRAM.

In Program mode, this command writes “OTP” data to SRAM for programming.

(10) Data Stop (DSP) (R11H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Stopping data transmission	0	0	0	0	0	1	0	0	0	1
	1	1	Data_flag	-	-	-	-	-	-	-

To stop data transmission, this command must be issued to check the data_flag.

Data_flag: Data flag of receiving user data.

0: Driver didn’t receive all the data.

1: Driver has already received all the one-frame data (DTM1 and DTM2).

After “Data Start” (R10h) or “Data Stop” (R11h) commands and when data_flag=1, the refreshing of panel starts and BUSY signal will become “0”.

(11) Display Refresh (DRF) (R12H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Refreshing the display	0	0	0	0	0	1	0	0	1	0

While user sent this command, driver will refresh display (data/VCOM) according to SRAM data and LUT.

After Display Refresh command, BUSY signal will become “0” and the refreshing of panel starts.

(12) Data Start Transmission 2 (DTM2) (R13H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Starting data transmission	0	0	0	0	0	1	0	0	1	1
	0	1	Pixel1	Pixel2	Pixel3	Pixel4	Pixel5	Pixel6	Pixel7	Pixel8
	0	1	..	..	..	..	..	..	..	..
	0	1	Pixel(n-7)	Pixel(n-6)	Pixel(n-5)	Pixel(n-4)	Pixel(n-3)	Pixel(n-2)	Pixel(n-1)	Pixel(n)

This command starts transmitting data and writes them into SRAM.

In B/W mode, this command writes “NEW” data to SRAM.

In B/W/Red mode, this command writes “RES” data to SRAM.

(13) VCOM LUT (LUTC) (R20H)

This command builds Look-up Table for VCOM

(14) W2W LUT (LUTWW) (R21H)

This command builds Look-up Table for White-to-White.

(15) B2W LUT (LUTBW/LUTR) (R22H)

This command builds Look-up Table for Black-to-White.

(16) W2B LUT (LUTWB/LUTW) (R23H)

This command builds Look-up Table for White - to- Black.

(17) B2B LUT (LUTBB / LUTB) (R24H)

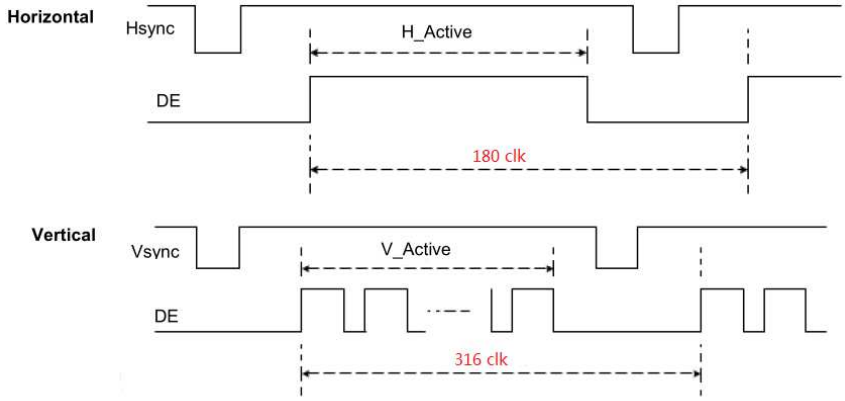
This command builds Look-up Table for Black - to- Black.

(18) PLL Control (PLL) (R30H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Controlling PLL	0	0	0	0	1	1	0	0	0	0
	0	1	-	-	M[2:0]			N[2:0]		

The command controls the PLL clock frequency. The PLL structure must support the following frame rates:

M	N	Frame Rate	M	N	Frame Rate	M	N	Frame Rate	M	N	Frame Rate
1	1	29 Hz	3	1	86 Hz	5	1	150 Hz	7	1	200 Hz
	2	14 Hz		2	43 Hz		2	72 Hz		2	100 Hz
	3	10 Hz		3	29 Hz		3	48 Hz		3	67 Hz
	4	7 Hz		4	21 Hz		4	36 Hz		4	50 Hz (Default)
	5	6 Hz		5	17 Hz		5	29 Hz		5	40 Hz
	6	5 Hz		6	14 Hz		6	24 Hz		6	33Hz
	7	4 Hz		7	12Hz		7	20 Hz		7	29 Hz
2	1	57 Hz	4	1	114 Hz	6	1	171 Hz			
	2	29 Hz		2	57 Hz		2	86 Hz			
	3	19 Hz		3	38 Hz		3	57 Hz			
	4	14 Hz		4	29Hz		4	43 Hz			
	5	11 Hz		5	23 Hz		5	34 Hz			
	6	10 Hz		6	19 Hz		6	29 Hz			
	7	8 Hz		7	16 Hz		7	24 Hz			



(19) Temperature Sensor Calibration (TSC) (R40H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Sensing Temperature	0	0	0	1	0	0	0	0	0	0
	1	1	D10/TS7	D9/TS6	D8/TS5	D7/TS4	D6/TS3	D5/TS2	D4/TS1	D3/TS0
	1	1	D2	D1	D0	-	-	-	-	-

This command reads the temperature sensed by the temperature sensor.

TS[7:0]: When TSE (R41h) is set to 0, this command reads internal temperature sensor value.

D[10:0]: When TSE (R41h) is set to 1, this command reads external LM75 temperature sensor value.

TS[7:0]/D[10:3]	Temperature (℃)	TS[7:0]/D[10:3]	Temperature (℃)	TS[7:0]/D[10:3]	Temperature (℃)
1110_0111	-25	0000_0000	0	0001_1001	25
1110_1000	-24	0000_0001	1	0001_1010	26
1110_1001	-23	0000_0010	2	0001_1011	27
1110_1010	-22	0000_0011	3	0001_1100	28
1110_1011	-21	0000_0100	4	0001_1101	29
1110_1100	-20	0000_0101	5	0001_1110	30
1110_1101	-19	0000_0110	6	0001_1111	31
1110_1110	-18	0000_0111	7	0010_0000	32
1110_1111	-17	0000_1000	8	0010_0001	33
1111_0000	-16	0000_1001	9	0010_0010	34
1111_0001	-15	0000_1010	10	0010_0011	35
1111_0010	-14	0000_1011	11	0010_0100	36
1111_0011	-13	0000_1100	12	0010_0101	37
1111_0100	-12	0000_1101	13	0010_0110	38
1111_0101	-11	0000_1110	14	0010_0111	39
1111_0110	-10	0000_1111	15	0010_1000	40

1111_0111	-9	0001_0000	16	0010_1001	41
1111_1000	-8	0001_0001	17	0010_1010	42
1111_1001	-7	0001_0010	18	0010_1011	43
1111_1010	-6	0001_0011	19	0010_1100	44
1111_1011	-5	0001_0100	20	0010_1101	45
1111_1100	-4	0001_0101	21	0010_1110	46
1111_1101	-3	0001_0110	22	0010_1111	47
1111_1110	-2	0001_0111	23	0011_0000	48
1111_1111	-1	0001_1000	24	0011_0001	49

(20) Temperature Sensor Enable (TSE) (R41H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Enable Temperature	0	0	0	1	0	0	0	0	0	1
Sensor/Offset	0	1	TSE	-	-	-	TO[3:0]			

This command selects Internal or External temperature sensor.

TSE: Internal temperature sensor switch

0: Enable (Default) 1: Disable; using external sensor.

TO[3:0]: Temperature offset.

TO[3:0]	Calculation	TO[3:0]	Calculation
0000 b	0	1000	-8
0001	1	1001	-7
0010	2	1010	-6
…	…	…	…
0110	6	1110	-2
0111	7	1111	-1

(21) Temperature Sensor Write (TSW) (R42H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Write External Temperature Sensor	0	0	0	1	0	0	0	0	1	0
	0	1	WATTR[7:0]							
	0	1	WMSB[7:0]							
	0	0	WLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

WATTR: D[7:6]: I^2C Write Byte Number

00b : 1 byte (head byte only)

01b : 2 bytes (head byte + pointer)

10b : 3 bytes (head byte + pointer + 1st parameter)

11b : 4 bytes (head byte + pointer + 1st parameter + 2nd parameter)

D[5:3]: User-defined address bits (A2, A1, A0)

D[2:0]: Pointer setting

WMSB[7:0]: MSByte of write-data to external temperature sensor.

WLSB[7:0]: LSByte of write-data to external temperature sensor.

(22) Temperature Sensor Read (TSR) (R43H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read External Temperature Sensor	0	0	0	1	0	0	0	0	1	1
	1	1	RMSB[7:0]							
	1	1	RLSB[7:0]							

This command reads the temperature sensed by the temperature sensor.

RMSB[7:0]: MSByte read data from external temperature sensor

RLSB[7:0]: LSByte read data from external temperature sensor

(23) VCOM And Data Interval Setting (CDI) (R50H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Interval Between Vcom and	0	0	0	1	0	1	0	0	0	0
Data	0	1	VBD[1:0]		DDX[1:0]		CDI[3:0]			

This command indicates the interval of Vcom and data output. When setting the vertical back porch, the total blanking will be kept (20 Hsync).

VBD[1:0]: Border data selection

B/W/Red mode (BWR=0)

DDX[0]	VBD[1:0]	LUT	DDX[0]	VBD[1:0]	LUT
0	00	Floating	1(Default)	00	LUTB
	01	LUTR		01	LUTW
	10	LUTW		10	LUTR
	11	LUTB		11	Floating

B/W mode (BWR=1)

DDX[0]	VBD[1:0]	LUT	DDX[0]	VBD[1:0]	LUT
0	00	Floating	1(Default)	00	Floating
	01	LUTBW (1→0)		01	LUTWB (1→0)
	10	LUTWB (0→1)		10	LUTBW (0→1)
	11	Floating		11	Floating

DDX[1:0]: Data polality.

DDX[1] for RED data, DDX[0] for BW data in the B/W/Red mode.

DDX[0] for B/W mode.

B/W/Red mode (BWR=0)

DDX[1:0]	Data{Red, B/W}	LUT	DDX[1:0]	Data{Red, B/W}	LUT
00	00	LUTW	10	00	LUTR
	01	LUTB		01	LUTR
	10	LUTR		10	LUTW
	11	LUTR		11	LUTB
01(Default)	00	LUTB	11	00	LUTR
	01	LUTW		01	LUTR
	10	LUTR		10	LUTB
	11	LUTR		11	LUTW

B/W mode (BWR=1)

DDX[0]	Data{New, Old}	LUT	DDX[0]	Data{New, Old}	LUT
0	00	LUTWW (0→0)	1(Default)	00	LUTBB (0→0)
	01	LUTBW (1→0)		01	LUTWB (0→1)
	10	LUTWB (0→1)		10	LUTBW (1→0)
	11	LUTBB (1→1)		11	LUTWW (1→1)

CDI[3:0]: Vcom and data interval

CDI[3:0]	Vcom and Data Interval	CDI[3:0]	Vcom and Data Interval
0000 b	17 hsync	0110	11
0001	16	0111	10 (Default)
0010	15	…	…
0011	14	1101	4
0100	13	1110	3
0101	12	1111	2

(24) Low Power Detection (LPD) (R51H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Detect Low Power	0	0	0	1	0	1	0	0	0	1
	1	1	-	-	-	-	-	-	-	LPD

This command indicates the input power condition. Host can read this flag to learn the battery condition.

LPD: Interval Low Power Detection Flag

0: Low power input (VDD < 2.5V) 1: Normal status (default)

(25) TCON Setting (TCON) (R60H)

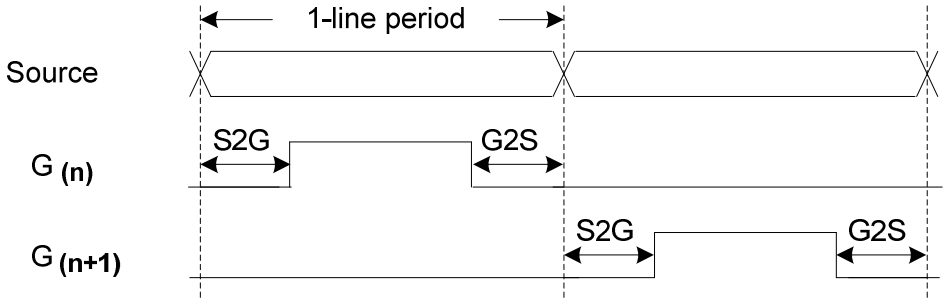
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Gate/Source Non-overlap	0	0	0	1	1	0	0	0	0	0
Period	0	1	S2G[3:0]				G2S[3:0]			

This command defines non-overlap period of Gate and Source.

S2G[3:0] or G2S[3:0]: Source to Gate / Gate to Source Non-overlap period

S2G[3:0] or G2S[3:0]	Period		S2G[3:0] or G2S[3:0]	Period
0000b	4		…	…
0001	8		1011	48
0010	12(Default)		1100	52
0011	16		1101	56
0100	20		1110	60
0101	24		1111	64

Period = 660 nS.



(26) Resolution Setting (TRES) (R61H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set Display Resolution	0	0	0	1	1	0	0	0	0	1
	0	1	HRES[7:3]					0	0	0
	0	1	-	-	-	-	-	-	-	VRES[8]
	0	0	VRES[7:0]							

This command defines alternative resolution and this setting is of higher priority than the RES[1:0] in R00H (PSR).

HRES[7:3]: Horizontal Display Resolution

VRES[8:0]: Vertical Display Resolution

Active channel calculation:

GD : First active gate = G0 (Fixed); LAST active gate = VRES[8:0] - 1

SD : First active source =S0 (Fixed); LAST active source = HRES[7:3]*8 – 1

(27) Revision (REV) (R70H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Chip Revision	0	0	0	1	1	1	0	0	0	0
	1	1	LUT_REV							

The LUT_REV is read from OTP address = 0x001.

(28) Get Status (FLG) (R71H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Read Flags	0	0	0	1	1	1	0	0	0	1
	1	1	-	PTL_flag	I^2C_ERR	I^2C_ BUSY	data_ flag	PON	POF	BUSY

This command reads the IC status.

PTL_FLAG Partial display status (high: partial mode)

I^2C_ERR: I^2C master error status

I^2C_BUSY: I^2C master busy status (low active)

data_flag: Driver has already received all the one frame data

PON: Power ON status

POF: Power OFF status

BUSY: Driver busy status (low active)

(29) Auto Measure Vcom (AMV) (R80H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	0
	0	1	-	-	AMVT[1:0]		XON	AMVS	AMV	AMVE

This command reads the IC status.

AMVT[1:0]: Auto Measure Vcom Time

00b: 3s 01b: 5s (Default)

10b: 8s 11b: 10s

XON: All Gate ON of AMV

0: Gate normally scan during Auto Measure VCOM period. (default)

1: All Gate ON during Auto Measure VCOM period.

AMVS: Source output of AMV

0: Source output 0V during Auto Measure VCOM period. (default)

1: Source output VDHR during Auto Measure VCOM period.

AMV: Analog signal

0: Get Vcom value with the VV command (R81h) (default)

1: Get Vcom value in analog signal. (External analog to digital converter)

AMVE: Auto Measure Vcom Enable (/Disable)

0: No effect

1: Trigger auto Vcom sensing.

(30) Vcom Value (VV) (R81H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Automatically measure Vcom	0	0	1	0	0	0	0	0	0	1
	1	1	-	-	VV[5:0]					

This command gets the Vcom value.

VV[5:0]: Vcom Value Output

VV[5:0]	Vcom value
00 0000b	-0.10 V
00 0001b	-0.15 V
00 0010b	-0.20 V
:	:
11 1010b	-3.00 V

(31) VCM_DC Setting (VDCS) (R82H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Set	0	0	1	0	0	0	0	0	1	0
VCM_DC	0	1	-	-	VDCS[5:0]					

This command sets VCOM_DC value

VDCS[5:0]: VCOM_DC Setting

VDCS[5:0]	Vcom value
00 0000b	-0.10 V (default)
00 0001b	-0.15 V
00 0010b	-0.20 V
:	:
11 1010b	-3.00 V

(32) Partial Window(PTL) (R90H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
	0	0	1	0	0	1	0	0	0	0
	0	1	HRST[7:3]					0	0	0
	0	1	HRED[7:3]					1	1	1
Set Partial	0	1	-	-	-	-	-	-	-	VRST[8]
Window	0	1	VRST[7:0]							
	0	1	-	-	-	-	-	-	-	VRED[8]
	0	1	VRED[7:0]							
	0	1	-	-	-	-	-	-	-	PT_SCAN

This command sets partial window.

HRST[7:3]: Horizontal start channel bank. (value 00h~13h)

HRED[7:3]: Horizontal end channel bank. (value 00h~13h). HRED must be greater than HRST.

VRST[8:0]: Vertical start line. (value 000h~127h)

VRED[8:0]: Vertical end line. (value 000h~127h). VRED must be greater than VRST.

PT_SCAN: 0: Gates scan only inside of the partial window.

1: Gates scan both inside and outside of the partial window. (default)

(33) Partial In (PTIN) (R91H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial In	0	0	1	0	0	1	0	0	0	1

This command makes the display enter partial mode.

(34) Partial Out (PTOUT) (R92H)

Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Partial In	0	0	1	0	0	1	0	0	1	0

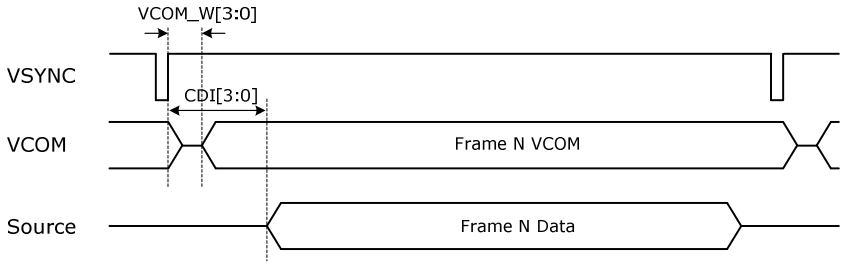
This command makes the display exit partial mode and enter normal mode.

(35) Power Saving (PWS) (RE3H)

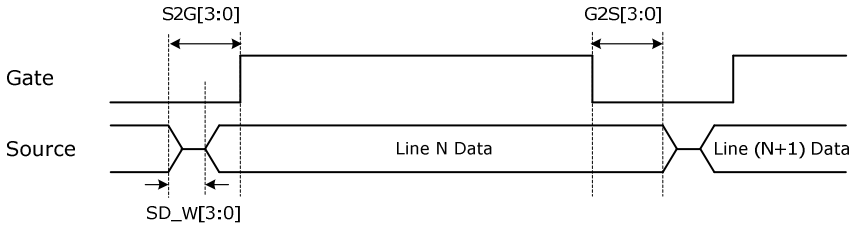
Action	W/R	C/D	D7	D6	D5	D4	D3	D2	D1	D0
Power Saving for	0	0	1	1	1	0	0	0	1	1
Vcom &Source	0	1	VCOM W[3:0]				SD W[3:0]			

This command is set for saving power during fresh period. If the output voltage of VCOM / Source is from negative to positive or from positive to negative, the power saving mechanism will be activated. The active period width is defined by the following two parameters.

VCOM_W[3:0]: VCOM power saving width (unit = line period)



SD_W[3:0]: Source power saving width (unit = 660nS)



7. Display Module Electrical Characteristics

7-1) Absolute Maximum Ratings:

Parameter	Symbol	Rating	Unit
Logic Supply Voltage	VDD	-0.3 to +6.0	V
Logic Input Voltage	V_{IN}	-0.3 to VDD +2.4	V
Operating Temp. range	T_{OPR}	0 to +50	℃
Storage Temp. range	T_{STG}	-25 to +70	℃

7-2) Display Module DC characteristics

The following specifications apply for: VSS = 0V, VDD = 3.3V, TA = 25℃

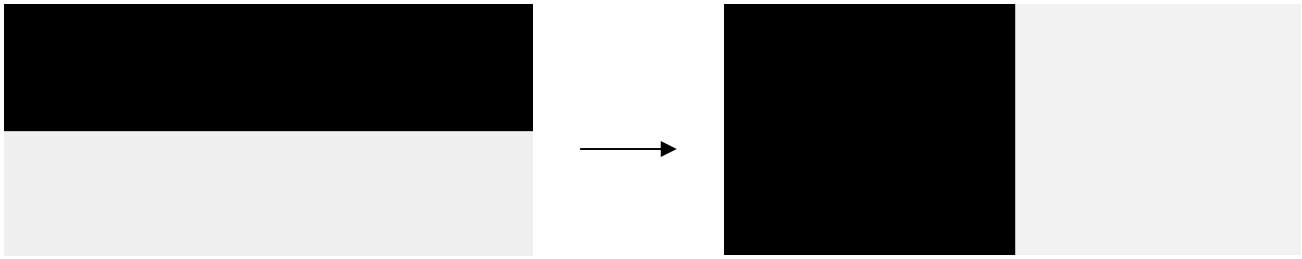
DIGITAL DC CHARACTERISTICS						
Symbol	**Parameter**	**Conditions**	**MIN.**	**TYP.**	**MAX.**	**Unit**
VDD	Logic supply voltage		2.3	3.3	3.6	V
VIL	Low level input voltage	Digital input pins	0	--	0.3XVDD	V
VIH	High level input voltage	Digital input pins	0.7xVDD	--	VDD	V
VOH	High level output voltage	Digital input pins, IOH=400 uA	VDD-0.4	--	--	V
VOL	Low level output voltage	Digital input pins, IOL=-400 uA	0	--	0.4	V
IMSTB	Module stand-by current	Shut-down mode	--	5		uA
IMDS	Module deep sleep current	Deep sleep mode		0.4	1	uA
IMOPR	Module operating current			8		mA
P	Operation Power Dissipation	VDD=3.3V with DC-DC		26.4		mW
PSTBY	Standby Power Dissipation	VDD=3.3V		16.5		uW

The Typical power consumption is measured with following pattern transition: from horizontal 2 gray scale pattern to vertical 2 gray scale pattern.(Note 7-1)

- The standby power is the consumed power when the panel controller is in standby mode.
- The listed electrical/optical characteristics are only guaranteed under the controller & waveform provided by WF
- Vcom is recommended to be set in the range of assigned value ± 0.1V.

Note 7-1

The Typical power consumption



7-3) Panel AC Characteristics

7-3-1) Oscillator frequency

The following specifications apply for : VSS = 0V, VDD = 3.3V, T_A = 25℃

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Internal Oscillator frequency	Fosc	VCI=2.7 to 3.6V	-	1.625	-	MHz

7-3-2) MCU Interface

7-3-2-1) MCU Interface Selection

In this module, there are 4-wire SPI and 3-wire SPI that can communicate with MCU. The MCU interface mode can be set by hardware selection on BS1 pins. When it is “Low”, 4-wire SPI is selected. When it is “High”, 3-wire SPI (9 bits SPI) is selected.

Pin Name	Data/Command Interface		Control Signal		
Bus interface	D1	D0	CS#	D/C#	RES#
SPI4	SDIN	SCLK	CS#	D/C#	RES#
SPI3	SDIN	SCLK	CS#	L	RES#

Table 7-1: MCU interface assignment under different bus interface mode

Note 7-2: L is connected to VSS

Note 7-3: H is connected to VCI

7-3-2-2) MCU Serial Interface (4-wire SPI)

The 4-wire SPI consists of serial clock SCLK, serial data SDIN, D/C#, CS#. In SPI mode, D0 acts as SCLK, D1 acts as SDIN.

Function	CS#	D/C#	SCLK
Write Command	L	L	↑
Write data	L	H	↑

Table 7-2: Control pins of 4-wire Serial Peripheral interface

Note 7-4: ↑stands for rising edge of signal

SDIN is shifted into an 8-bit shift register in the order of D7, D6, ... D0. The data byte in the shift register is written to the Graphic Display Data RAM (RAM) or command register in the same clock. Under serial mode, only write operations are allowed.

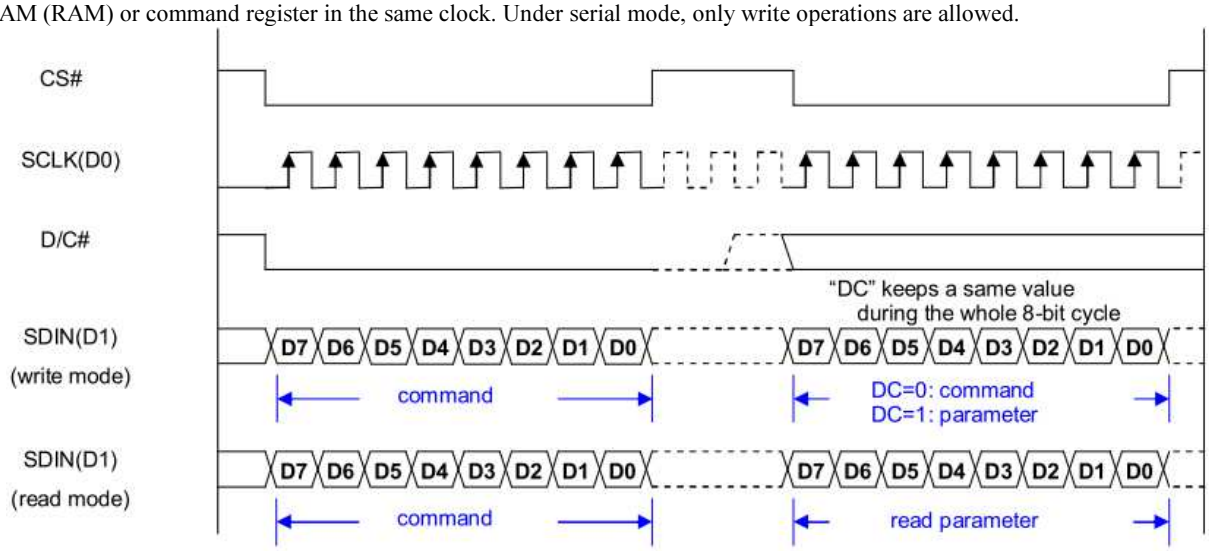


Figure 7-1: Write procedure in 4-wire Serial Peripheral Interface mode

7-3-2-3) MCU Serial Interface (3-wire SPI)

The 3-wire serial interface consists of serial clock SCLK, serial data ADIN and CS#.

In 3-wire SPI mode, D0 acts as SCLK, D1 acts as SDIN, The pin D/C# can be connected to an external ground.

The operation is similar to 4-wire serial interface while D/C# pin is not used. There are altogether 9-bits will be shifted into the shift register on every ninth clock in sequence: D/C# bit, D7 to D0 bit. The D/C# bit (first bit of the sequential data) will determine the following data byte in shift register is written to the Display Data RAM (D/C# bit = 1) or the command register (D/C# bit = 0).Under serial mode, only write operations are allowed.

Function	CS#	D/C#	SCLK
Write Command	L	Tie LOW	↑
Write data	L	Tie LOW	↑

Table 7-3: Control pins of 3-wire Serial Peripheral Interface

Note 7-5: ↑stands for rising edge of signal

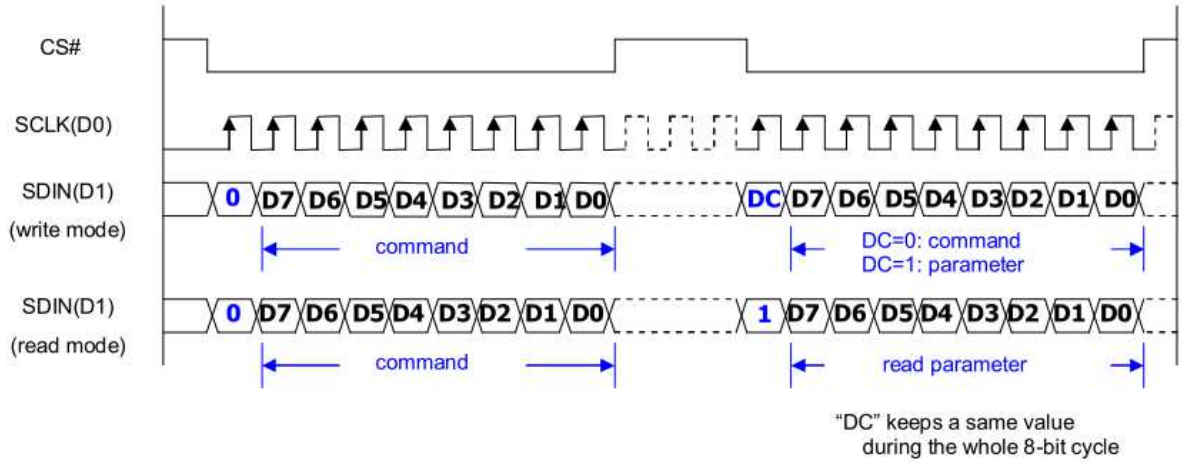
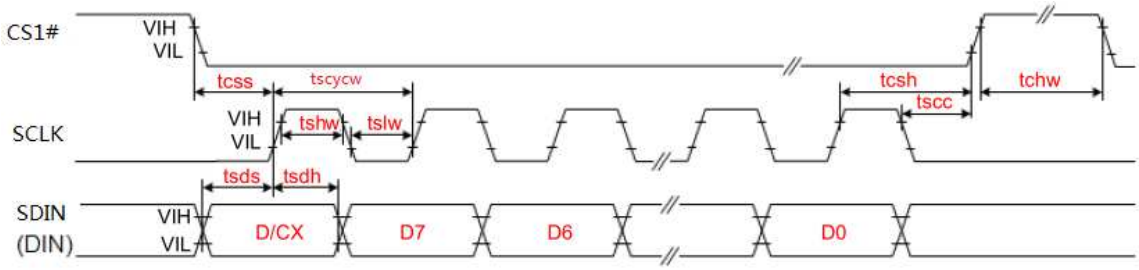
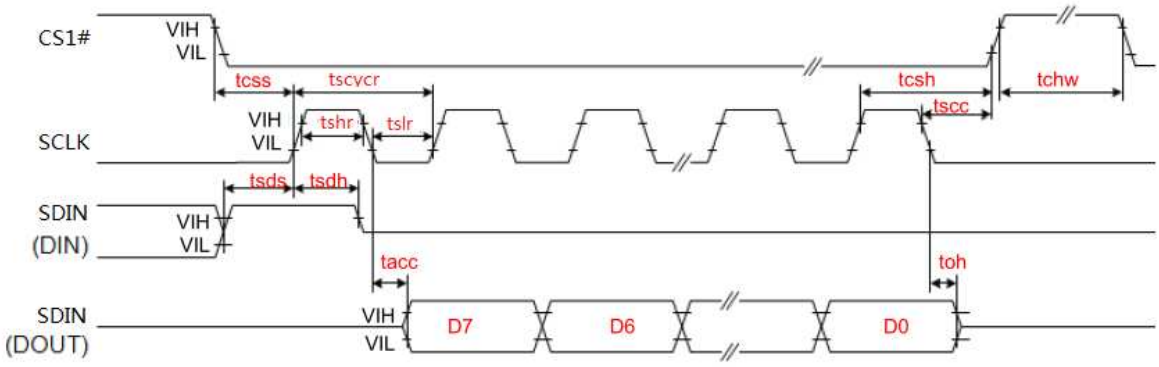


Figure 7-2: Write procedure in 3-wire Serial Peripheral Interface mode

7-3-3) Timing Characteristics of Series Interface



3-wire Serial Interface – Write



3-wire Serial Interface – Read

Symbol	Signal	Parameter	Min	Typ	Max	Unit
tcss	CS#	Chip Select Setup Time	60	-	-	ns
tcsh		Chip Select Hold Time	65	-	-	ns
tscc		Chip Select Setup Time	20	-	-	ns
tchw		Chip Select Setup Time	40	-	-	ns
tscycw	SCL	Serial clock cycle (write)	100	-	-	ns
tshw		SCL “H” pulse width (write)	35	-	-	ns
tslw		SCL“L” pulse width (write)	35	-	-	ns
tscycr		Serial clock cycle (Read)	150	-	-	ns
tshr		SCL “H” pulse width (Read)	60	-	-	ns
tslr		SCL “L” pulse width (Read)	60	-	-	ns
tsds	SDIN (DIN) (DOUT)	Data setup time	30	-	-	ns
tsdh		Data hold time	30	-	-	ns
tacc		Access time	-	-	10	ns
toh		Output disable time	15	-	-	ns

7-4) Power Consumption

Parameter	Symbol	Conditions	TYP	Max	Unit	Remark
Panel power consumption during update	-	25℃	26.4		mW	-
Power consumption in standby mode	-	25℃	16.5		uW	-

7-5) Reference Circuit

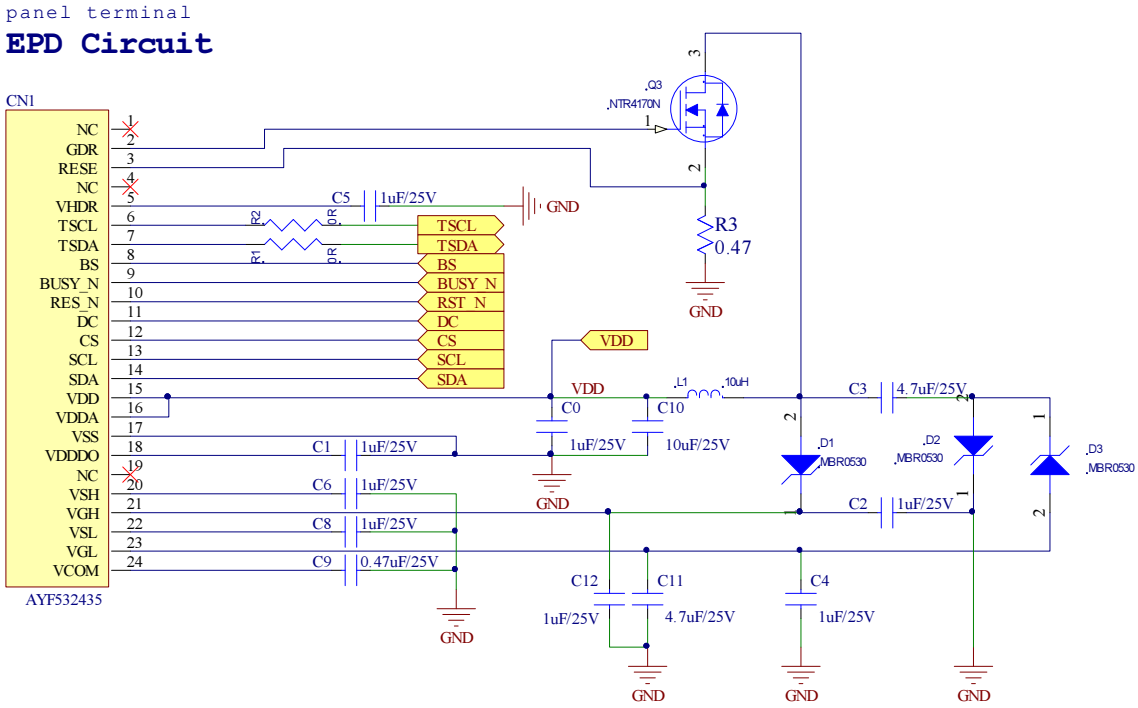


Figure . 7-5 (1)

8. Optical characteristics

8-1) Specifications

Measurements are made with that the illumination is under an angle of 45 degrees, the detector is perpendicular unless otherwise specified.

T = 25°C

Symbol	Parameter	Conditions	Min	Typ.	Max	Unit	Note
R	Reflectance	White	30	35	-	%	Note 9-1
CR	Contrast Ratio	-	8	10	-		-

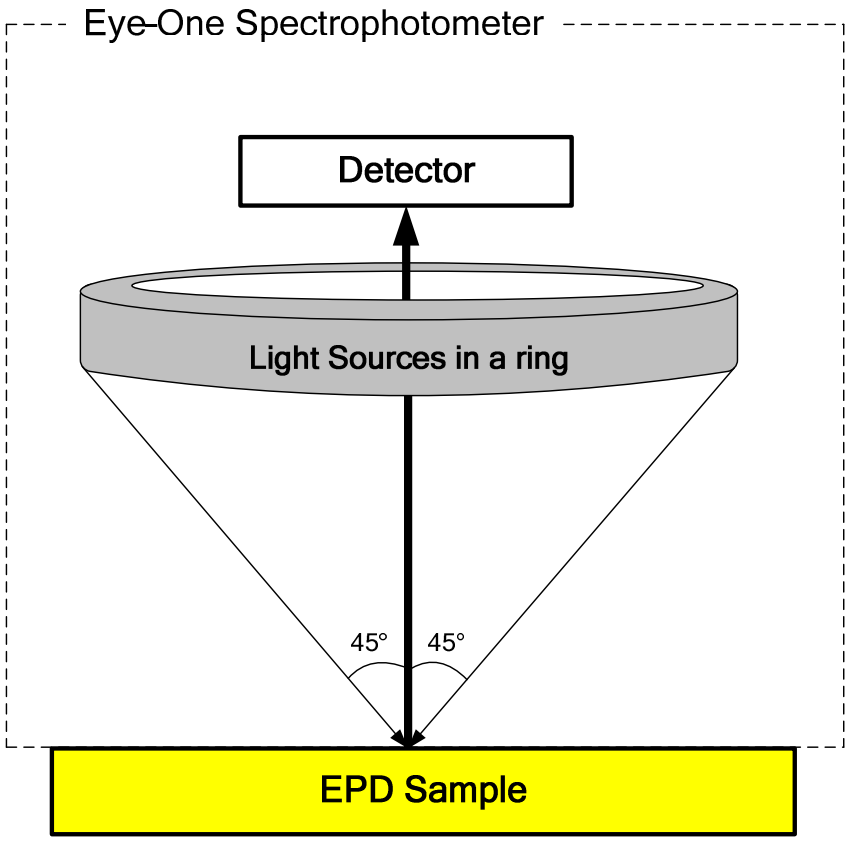
WS：White state , DS：Dark state

Note 8-1：Luminance meter：Eye – One Pro Spectrophotometer

8-2) Definition of contrast ratio

The contrast ratio (CR) is the ratio between the reflectance in a full white area (Rl) and the reflectance in a dark area (Rd)：

CR = Rl/Rd



8-3) Reflection Ratio

The reflection ratio is expressed as：

$R = \text{Reflectance Factor}_{\text{white board}} \quad x \quad (L_{\text{center}} / L_{\text{white board}})$

L_{center} is the luminance measured at center in a white area . $L_{\text{white board}}$ is the luminance of a standard white board. Both are measured with equivalent illumination source. The viewing angle shall be no more than 2 degrees.

9. HANDLING, SAFETY AND ENVIROMENTAL REQUIREMENTS:

WARNING
The display glass may break when it is dropped or bumped on a hard surface. Handle with care. Should the display break, do not touch the electrophoretic material. In case of contact with electrophoretic material, wash with water and soap.

CAUTION
The display module should not be exposed to harmful gases, such as acid and alkali gases, which corrode electronic components.
Disassembling the display module can cause permanent damage and invalidate the warranty agreements.
IPA solvent can only be applied on active area and the back of a glass. For the rest part, it is not allowed.

Mounting Precautions
(1) It`s recommended that you consider the mounting structure so that uneven force (ex. Twisted stress) is not applied to the module.
(2) It`s recommended that you attach a transparent protective plate to the surface in order to protect the EPD. Transparent protective plate should have sufficient strength in order to resist external force.
(3) You should adopt radiation structure to satisfy the temperature specification.
(4) Acetic acid type and chlorine type materials for the cover case are not desirable because the former generates corrosive gas of attacking the PS at high temperature and the latter causes circuit break by electro-chemical reaction.
(5) Do not touch, push or rub the exposed PS with glass, tweezers or anything harder than HB pencil lead. And please do not rub with dust clothes with chemical treatment. Do not touch the surface of PS for bare hand or greasy cloth. (Some cosmetics deteriorate the PS)
(6) When the surface becomes dusty, please wipe gently with absorbent cotton or other soft materials like chamois soaks with petroleum benzene. Normal-hexane is recommended for cleaning the adhesives used to attach the PS. Do not use acetone, toluene and alcohol because they cause chemical damage to the PS.
(7) Wipe off saliva or water drops as soon as possible. Their long time contact with PS causes deformations and color fading.

Data sheet status	
Product specification	This data sheet contains final product specifications subjected to changes without notice.

Limiting values

Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information

Where application information is given, it is advisory and does not form part of the specification.

10. Reliability test

	TEST	CONDITION	REMARK
1	High Temperature Storage	Ta= 70°C 40% RH, 240Hrs	(Test in White Pattern)
2	Low Temperature Storage	Ta= -25°C, 240Hrs	(Test in White Pattern)
3	High Temperature Operation	Ta= 50°C 30% RH, 240Hrs	
4	Low Temperature Operation	Ta= 0°C, 240Hrs	
5	High Temperature High Humidity Operational test	Ta= 40°C 80% RH, 240Hrs	
6	High Temperature High Humidity Storage test	Ta= 60°C 80% RH, 240Hrs	(Test in White Pattern)
7	Thermal cycles	-25°C(30min) ~60°C (30min), 50 cycle, 1Hr/cycle	(Test in White Pattern)
8	Solar radiation test	765 W/m^2 for 168hrs,40℃	(Test in White Pattern)
9	Electrostatic Discharge	(Machine model) +/- 200V 0Ω , 200pF	Non-operation

Actual EMC level to be measured on customer application.

Note：The protective film must be removed before temperature test.

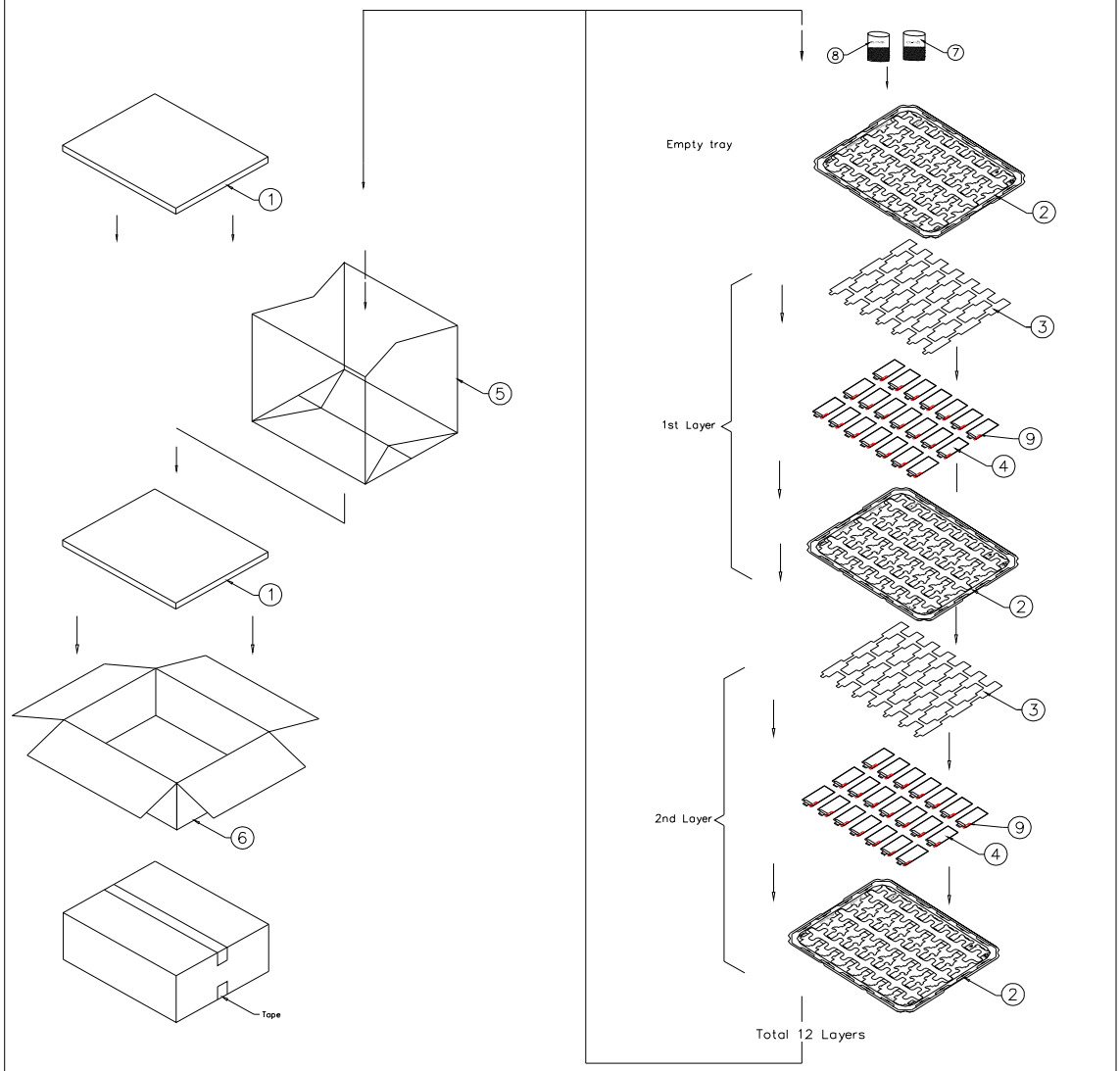
< Criteria >

In the standard conditions, there is not display function NG issue occurred.

All the cosmetic specification is judged before the reliability stress.

11. Packing

REV	DESCRIPTION	DESIGN	DATE
10	INITIAL RELEASE	SY Lin	2016/04/14



NOTE:

1. One layer include: 1 piece of cushion sheet, 21 pcs module & 1 piece of tray.
2. Q'TY: 252 pcs panel/carton.
3. Dimension: 445*365*170mm
4. Weight: 5KG
5. Make sure tray stacked with 0° rotation. We can check this by lateral side view.

ITEM	DESCRIPTION	QTY	REMARK
9	Peeling tape	252	
8	30g加厚複合紙吸濕劑73*95mm	2	
7	防鏽劑(保護容積25L)	3	
6	CARTON INTERNAL	1	
5	摺口袋450*380*580mm	1	抗靜電
4	ED029TC1	252	
3	EPE CUSHION SHEET	12	抗靜電
2	TRAY	13	抗靜電
1	EPE FOAM	2	

MTL.SPEC.	UNSPECIFIED TOL'S ±5.0mm ANGLE ROUGHNESS	REMARK	E Ink 元太科技工業股份有限公司			
APPROVE	Patrick Lin	2016/4/14	SCALE 1:1	UNIT mm	SHEET 1 OF 1	DWG.TITLE ED029TC1 PACKING
CHECK	Patrick Lin	2016/4/14	MTL.NO.	DWG.NO.	REV.	A4 SIZE
DESIGN	SY Lin	2016/4/14				

12.Block Diagram