

# AIO-T USER'S GUIDE

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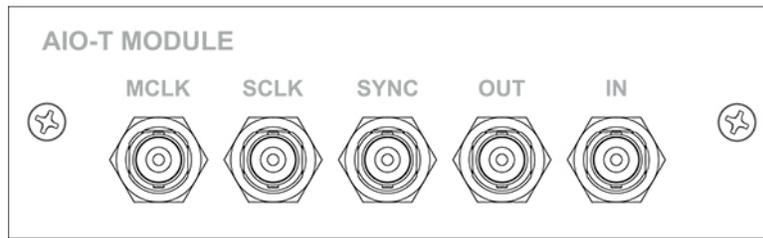


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The AIO-T module provides a digital TDM (Time-Division Multiplexed) interface for connection directly to audio converters or other ICs. Four outputs (MCLK, SCLK, SYNC, and OUT) and one input (IN) are provided on BNC connectors. The module functions as a TDM master, sourcing the clocks and synchronization signals.

### **AIO-T Hardware**

Five digital signals are provided on the AIO-T module using BNC connectors:



**IN** – Data input, can contain up to 10 channels of 24-bit audio input data

**OUT** – Data output, can contain up to 10 channels of 24-bit audio output data

**SYNC** – Frame synchronization output. Used to signal the start of an audio frame. Width, polarity, and phase relationship to the audio data are programmable.

**SCLK** – Bit clock output. Polarity and bits per frame are programmable. SCLK may also be set to be disabled, outputting a constant “0” logic level.

**MCLK** – 24.576 MHz master clock output.

### **Logic Levels**

A jumper on the AIO-T PCB sets the I/O logic levels to either 1.8V or 3.3V:

1.8V  3.3V  
TDM VOLTAGE

When termination is enabled (see below) only 1.8V should be used.

## Termination

Unless termination has been enabled in the AIO-T control register, outputs have minimal drive capability and a 22 ohm series resistance, while the data input has a high impedance.

When termination is enabled both the input and outputs are configured for 50 ohm termination. Logic “1” levels drive the outputs at 3.6V through a 50 ohm series resistance. This requires a corresponding 50 ohm resistor to ground at the connected device to divide this down to a proper 1.8V level. The data input of the AIO-T also has a 50 ohm termination resistor to ground when enabled.

## AIO-T Configuration

A microcontroller is built into the AIO-T module that controls all of the TDM transfers. There is no firmware storage on-board, so after powering up the AIO the firmware for this controller needs to be downloaded from the host computer. Once loaded, there are three 16-bit registers available for setting the various TDM options or reading the firmware version.

The AIO-T module will always show up as ten input channels and ten output channels on the host computer (along with channels for the other installed module). This is regardless of how the TDM interface is configured. These will appear to software as TDM 1, TDM 2, TDM 3, etc. If the TDM interface is set for fewer than ten channels, the lowest TDM channels are used and the higher channels are ignored.

Please note:

1. Data is limited to 24 bits and will be left justified within a 32 bit TDM word.
2. All registers may be read at any time.
3. TDM is disabled when firmware is first loaded.
4. Control Register (0x01) must be written before the Fsync Format Register (0x02).
5. If running, writing the Control Register will stop TDM transfers.
6. Writing the Fsync Format Register will initiate TDM transfers.
7. SCLK will start four frames in advance of FSYNC and DATA.

## Register Definitions

Address	Function	D15	D14	D13	D12	D11	D10	D9	D8	
0x00 (RO)	Firmware Version	MAJOR [7:0]								
		D7	D6	D5	D4	D3	D2	D1	D0	
		MINOR [7:0]								

Major [7:0]/Minor [7:0]: Version of currently loaded firmware.

Address	Function	D15	D14	D13	D12	D11	D10	D9	D8
0x01 (R/W)	Control	----	----	----	----	----	----	----	TERM_EN
		D7	D6	D5	D4	D3	D2	D1	D0
		INPUT_DLY	SCLK_EN	SCLK_POL	SYNC_DEL	FRAME [1:0]		WORD [1:0]	

TERM\_EN: Enables 3.6V drive with 50 ohm in series on outputs, 50 ohm termination on inputs  
0: Termination disabled  
1: Termination enabled

INPUT\_DLY: Input Delay  
0: No delay.  
1: TDM input is delayed by one bit.

SCLK\_EN: Enables SCLK output on the BNC connector  
0: A logic "0" is output  
1: TDM bit clock is output

SCLK\_POL: Determines which edge of SCLK is used for output  
0: Data and FSYNC change on the falling edge of SCLK  
1: Data and FSYNC change on the rising edge of SCLK

SYNC\_DEL: Determines if FSYNC clocks out along with data or is delayed by 1/2 SCLK cycle  
0: FSYNC clocks out along with data  
1: FSYNC is delayed by 1/2 SCLK cycle

FRAME [1:0]: Sets the number of bits per TDM frame  
00: 32 bits/frame (not implemented)  
01: 64 bits/frame (not implemented)  
10: 128 bits/frame (not implemented)  
11: 256 bits/frame

WORD [1:0]: Sets the number of bits per TDM word  
00: 8 bits/word (not implemented)  
01: 16 bits/word (not implemented)  
10: 24 bits/word  
11: 32 bits/word

Address	Function	D15	D14	D13	D12	D11	D10	D9	D8
0x02	FSYNC Format	WIDTH [7:0]							
		D7	D6	D5	D4	D3	D2	D1	D0
		POSITION [7:0]							

WIDTH [7:0]: FSYNC width. Valid FSYNC widths are 1 through BitsPerFrame/2

POSITION [7:0]: Bit position for start of positive portion of FSYNC. Valid positions are 0 (first data bit position) through BitsPerFrame - 1

## TDM Utility

Loading the AIO-T firmware and configuring up the TDM interface is done using the command line utility “tdm”. This may be run from another program, a script, or from within a Terminal (Command Prompt) window.

Address and register data are interpreted as hex values. For example, “0” is the same as “0x00” and “2fe” is equivalent to “0x02fe”.

The tdm utility performs four basic functions:

**Load:** Resets the AIO-T controller downloads the specified firmware.

Usage: tdm load filename

Example: tdm load AIO-T\_0x0108.bin

**Read:** Reads the register at the specified address.

Usage: tdm r address

Example: tdm r 0 (reads register 0x00)

**Write:** Writes the register at the specified address with the supplied data.

Usage: tdm w address data or

tdm w address=data address=data

Example: tdm w 1 cc (writes 0xcc into register 0x01)

tdm w 1=cc 2=ee (writes 0xcc into register 0x01 and 0xee into register 2)

**Reset:** Resets the controller on the AIO-T module. All clocks and data transfers over TDM will cease.

Usage: tdm reset

Please note:

1. macOS terminal commands need to be preceded with “.\”.
2. When running from Windows, tusbaudioapi.dll and custom.ini must be in the same directory as tdm.exe. These may be found in the directory specified when installing the AIO driver, typically C:\Program Files\Echo AIO\.