About JTAG Live CoreCommander

Benefits

- Overcomes deficiencies in boundary-scan registers
- Works with devices not compliant to IEEE std 1149.x
- Most popular processor cores supported (ARM PPC etc.)
- Code compatible with Python for test scripting
- Low-cost compared to other solutions.

Applications

CoreCommander routines can be used to boost test coverage in applications that have only a small amount or even no IEEE std 1149.1 (conventional boundary-scan) test access options. By taking hold directly of the target processor's core the user can write to or read from configuration registers and internal or external memory spaces.

Features

- Supported by JTAG Technologies, JTAG Live and FTDI based controllers/interfaces
- Simple to use interactive GUI to perform core writes/reads
- Functions include 'EnterDebug', 'ExitDebug', 'LoadMemory', 'SaveMemory', 'WritePC', 'ReadPC'
- Compatible with Python open-source scripting language.
- Works in tandem with JTAG Live Script – boundary-scan routines.