

PGY-RFFE-EX-PD

RFFE Exerciser and Protocol Analyzer



RFFE Protocol Analyzer (PGY-RFFE-EX-PD) is the Protocol Analyzer with multiple features to capture and debug communication between host and design under test. The RF Front-end control interface (RFFE) Serial bus interface is emerging as a chosen for controlling RF front end devices. There are a variety of front end devices such as Power Amplifiers (PA), Low-Noise Amplifiers (LNA), filters, switches, power management modules, antenna tuners. It is widely used in mobile devices.

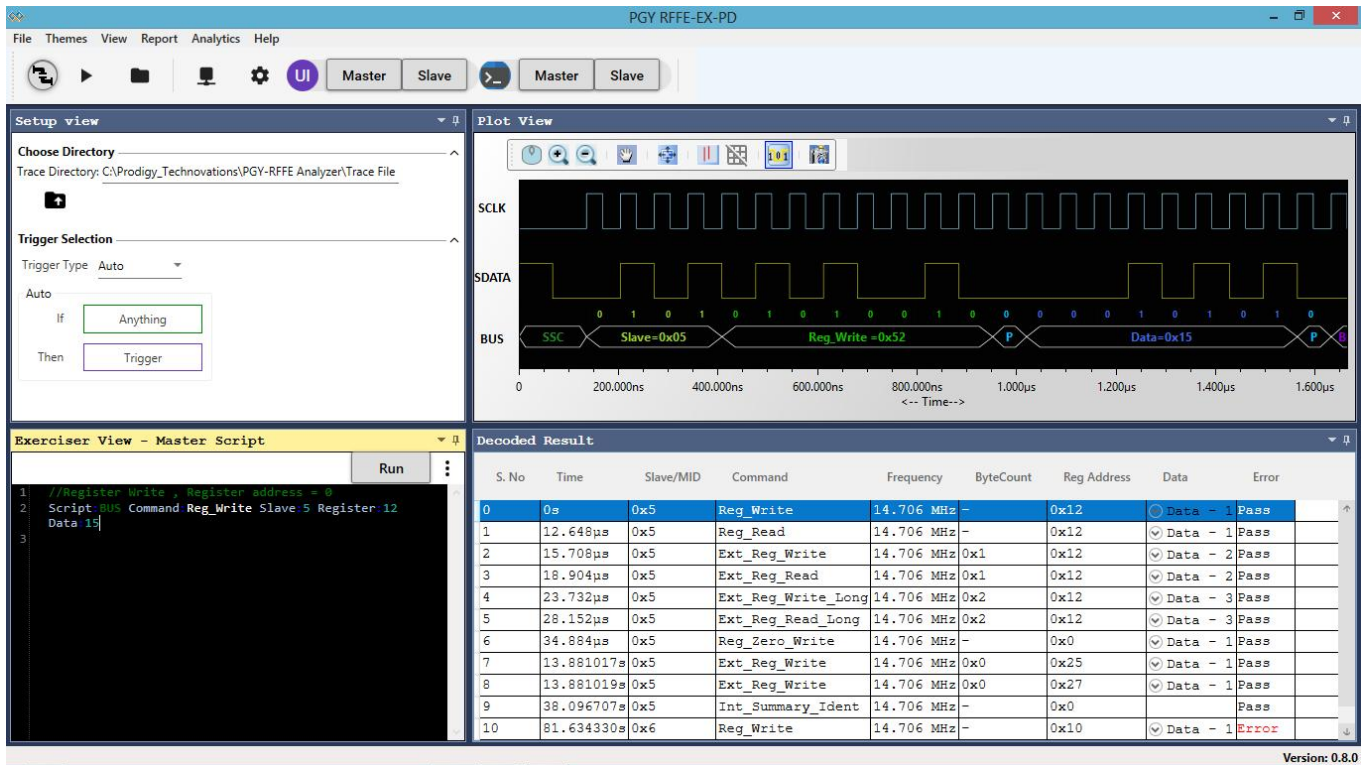
PGY-RFFE-EX-PD is the leading instrument that enables the design and test engineers to test the RFFE interface for its specifications by configuring PGY-RFFE-EX-PD as master/slave, generating RFFE traffic with error injection capability, amplitude variation, and decoding RFFE Protocol decode packets.

Key Features

- ❖ Supports RFFE2.0/2.1 Specification.
- ❖ Ability to configure it as Master or Slave.
- ❖ Generate different RFFE at full speed and half of full frequency speed.
- ❖ Error Injection such as parity errors and ACK/NACK errors.
- ❖ Variable RFFE data speeds.
- ❖ Simultaneously generate RFFE traffic and Protocol decode of the Bus.
- ❖ Timing diagram of the Protocol decoded bus.
- ❖ Listing view of Protocol activity.
- ❖ Error Analysis in Protocol Decode.
- ❖ Ability to write exerciser script to combine multiple data frame generation at different data speeds.
- ❖ USB2/3 host computer interface.
- ❖ Flexibility to upgrade to the unit for evolving RFFE Specification.

Multi-Domain view

Multi-domain View provides the complete view of RFFE Protocol activity in a single GUI. Users can easily set up the analyzer to generate RFFE traffic using a GUI or script. Users can set different trigger conditions from the setup menu to capture Protocol activity at specific events and decode the protocol transactions between Master and Slave. The decoded results can be viewed in the timing diagram and Protocol listing window with autocorrelation. This comprehensive view of information makes it the industry's best, offering an easy-to-use solution to debug the RFFE protocol activity.

The screenshot displays the PGY RFFE-EX-PD software interface. The top menu includes File, Themes, View, Report, Analytics, and Help. Below the menu are control buttons for Master and Slave, and a Run button. The interface is divided into four main sections:

- Setup view:** Shows the trace directory as C:\Prodigy_Technovations\PGY-RFFE Analyzer\Trace File. The Trigger Selection is set to Auto, with a condition 'If Anything' and a 'Then Trigger' action.
- Plot View:** A timing diagram showing SCLK, SDATA, and BUS signals. The BUS signal shows a sequence of operations: SSC, Slave=0x05, Reg_Write=0x52, P, and Data=0x15.
- Exerciser View - Master Script:** A script editor with a 'Run' button. The script contains the following commands:


```

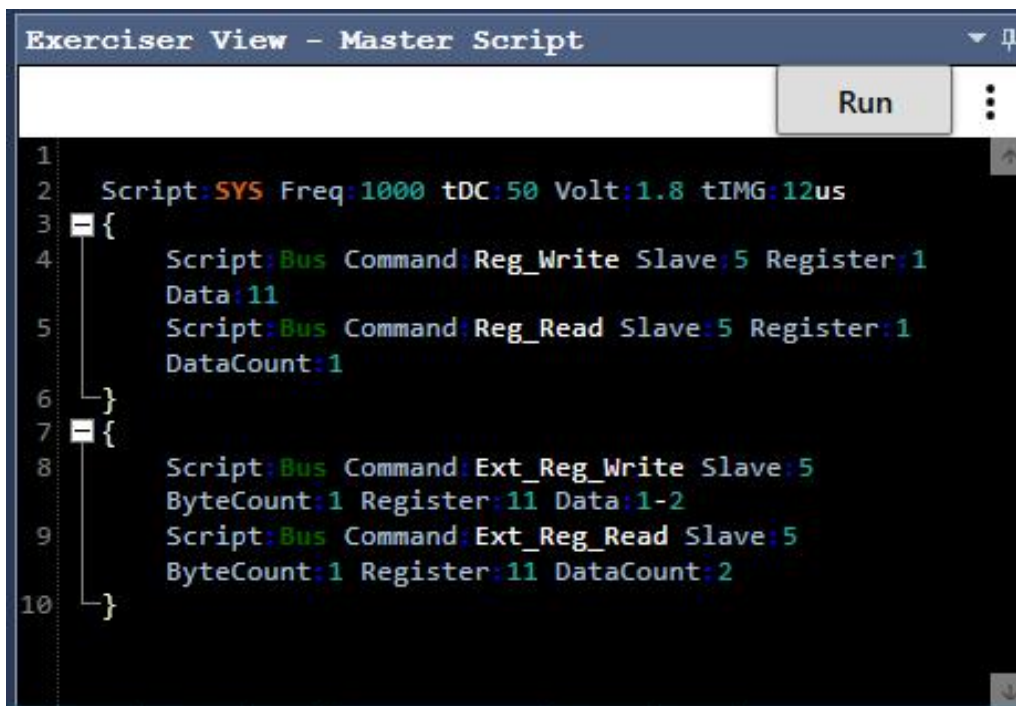
1 //Register Write , Register address = 0
2 Script:BUS Command:Reg_Write Slave:5 Register:12
  Data:15
3

```
- Decoded Result:** A table showing the execution results of the script.

| S.No | Time | Slave/MID | Command | Frequency | ByteCount | Reg Address | Data | Error |
|------|------------|-----------|--------------------|------------|-----------|-------------|----------|-------|
| 0 | 0s | 0x5 | Reg_Write | 14.706 MHz | - | 0x12 | Data - 1 | Pass |
| 1 | 12.648µs | 0x5 | Reg_Read | 14.706 MHz | - | 0x12 | Data - 1 | Pass |
| 2 | 15.708µs | 0x5 | Ext_Reg_Write | 14.706 MHz | 0x1 | 0x12 | Data - 2 | Pass |
| 3 | 18.904µs | 0x5 | Ext_Reg_Read | 14.706 MHz | 0x1 | 0x12 | Data - 2 | Pass |
| 4 | 23.732µs | 0x5 | Ext_Reg_Write_Long | 14.706 MHz | 0x2 | 0x12 | Data - 3 | Pass |
| 5 | 28.152µs | 0x5 | Ext_Reg_Read_Long | 14.706 MHz | 0x2 | 0x12 | Data - 3 | Pass |
| 6 | 34.884µs | 0x5 | Reg_Zero_Write | 14.706 MHz | - | 0x0 | Data - 1 | Pass |
| 7 | 13.881017s | 0x5 | Ext_Reg_Write | 14.706 MHz | 0x0 | 0x25 | Data - 1 | Pass |
| 8 | 13.881019s | 0x5 | Ext_Reg_Write | 14.706 MHz | 0x0 | 0x27 | Data - 1 | Pass |
| 9 | 38.096707s | 0x5 | Int_Summary_Ident | 14.706 MHz | - | 0x0 | | Pass |
| 10 | 81.634330s | 0x6 | Reg_Write | 14.706 MHz | - | 0x10 | Data - 1 | Error |

Version: 0.8.0

Exerciser



The screenshot shows the 'Exerciser View - Master Script' window. The script is as follows:

```

1
2 Script:SYS Freq:1000 tDC:50 Volt:1.8 tIMG:12us
3 {
4   Script:Bus Command:Reg_Write Slave:5 Register:1
  Data:11
5   Script:Bus Command:Reg_Read Slave:5 Register:1
  DataCount:1
6 }
7 {
8   Script:Bus Command:Ext_Reg_Write Slave:5
  ByteCount:1 Register:11 Data:1-2
9   Script:Bus Command:Ext_Reg_Read Slave:5
  ByteCount:1 Register:11 DataCount:2
10 }

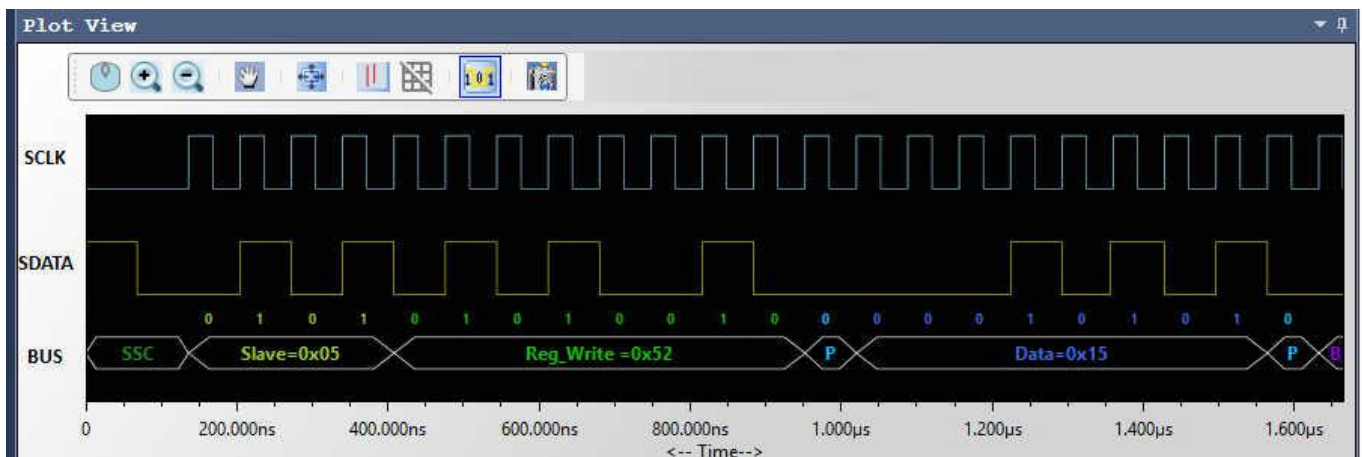
```

PGY-RFFE-EX-PD supports RFFE traffic generation using GUI and Script. Users can generate simple traffic generation using the GUI to test the DUT. Script-based GUI provides flexibility to emulate the complete expected traffic in the real-world including error injections. In this sample script user can generate RFFE traffic as below:



- ❖ Script line #4: REG Write to the slave with USID 5
- ❖ Script line #5: REG Read to the slave with USID 5
- ❖ Script line #8: EXT REG Write to the slave with USID 5
- ❖ Script line #9: EXT REG Read to the slave with USID 5

Timing Diagram and Protocol Listing View



The timing view provides the plot of SCLK and SDATA signals with a bus diagram. Overlaying of Protocol bits on the digital timing waveform will help easy debugging of Protocol decoded data. Cursor and Zoom features will make it convenient to analyze Protocol in the timing diagram for any timing errors.

| S. No | Time | Slave/MID | Command | Frequency | ByteCount | Reg Address | Data | Error |
|-------|------------|-----------|--------------------|------------|-----------|-------------|----------|-------|
| 0 | 0s | 0x5 | Reg_Write | 14.706 MHz | - | 0x12 | Data - 1 | Pass |
| 1 | 12.648µs | 0x5 | Reg_Read | 14.706 MHz | - | 0x12 | Data - 1 | Pass |
| 2 | 15.708µs | 0x5 | Ext_Reg_Write | 14.706 MHz | 0x1 | 0x12 | Data - 2 | Pass |
| 3 | 16.904µs | 0x5 | Ext_Reg_Read | 14.706 MHz | 0x1 | 0x12 | Data - 2 | Pass |
| 4 | 23.732µs | 0x5 | Ext_Reg_Write_Long | 14.706 MHz | 0x2 | 0x12 | Data - 3 | Pass |
| 5 | 28.152µs | 0x5 | Ext_Reg_Read_Long | 14.706 MHz | 0x2 | 0x12 | Data - 3 | Pass |
| 6 | 34.884µs | 0x5 | Reg_Zero_Write | 14.706 MHz | - | 0x0 | Data - 1 | Pass |
| 7 | 13.881017s | 0x5 | Ext_Reg_Write | 14.706 MHz | 0x0 | 0x25 | Data - 1 | Pass |
| 8 | 13.881019s | 0x5 | Ext_Reg_Write | 14.706 MHz | 0x0 | 0x27 | Data - 1 | Pass |
| 9 | 38.096707s | 0x5 | Int_Summary_Ident | 14.706 MHz | - | 0x0 | | Pass |
| 10 | 81.634330s | 0x6 | Reg_Write | 14.706 MHz | - | 0x10 | Data - 1 | Error |

The protocol window provides the decoded packet information in each state and all packet details. The selected frame in the Protocol listing window will be auto-correlated in the timing view to view the timing information of the packet.

Powerful Trigger Capabilities

Trigger Selection

Trigger Type **Advanced** ▾

Level Count **2** ▾

Level # 0

If

Broadcast S 0x7E W ACK ENTDAAs T

Directed Data T

Private

Then Action **Trigger** ▾

Else If

Broadcast S 0x7E W ACK SETMWL T

Directed Data 1-2 T

Private

Then Action **Nothing** ▾ Go to Level **1** ▾

PGY-RFFE-EX-PD supports auto, simple, and advanced trigger capabilities. The analyzer can trigger on any of the Protocol packets such as Ext. Reg. Write, Ext. Reg, read and so forth message. Advanced Trigger provides the flexibility to monitor multiple trigger conditions and can set multiple state trigger machines.

Specifications

| PGY-RFFE Specifications | Features | PGY-RFFE-EX-PD |
|----------------------------|------------------------------------|----------------|
| Exerciser: | | |
| Configurable | 1 Master + 4 Slaves | ✓ |
| RFFE Traffic Generation | Custom RFFE Traffic Generation | ✓ |
| SCL Frequency | 32KHz to 52 MHz (45?) | ✓ |
| Voltage Drive Level | 1.2V and 1.8V | ✓ |
| SCL duty cycle variation | 25%, 50% and 75% | ✓ |
| SCL and SDA delay | User defined in multiples of 5.2ns | ✓ |
| Delay between two messages | User defined | ✓ |

| | | |
|---------------------------|---|---|
| Error injection | Parity error injection | ✓ |
| Protocol Analysis: | | |
| Supports | RFFE 2.0/2.1 protocol decode | ✓ |
| Protocol Views | Timing Diagram View Protocol Listing View Bus-Diagram to display Protocol packets with timing diagram plot | ✓ |
| Protocol Trigger | Auto (Trigger on any packet) Simple (Trigger on any user defined RFFE packet) Advanced (Multi-state & multi-level trigger capability) | ✓ |
| Capture Duration | Continuous streaming Protocol Data | ✓ |
| Protocol Error Report | Parity | ✓ |
| Host Connectivity | USB 3.0 / 2.0 interface | ✓ |

Ordering Information

PGY-RFFE-EX-PD (v 2.0): RFFE Protocol Exerciser and Analyzer (v 2.0 specification supported)

PGY-RFFE-EX-PD (v2.1): RFFE Protocol Exerciser and Analyzer (v 2.1 specification supported)

PGY-RFFE-UPG (v2.0 to v 2.1): RFFE Protocol Exerciser and Analyzer (upgrade option from v 2.0 specification to v 2.1 specification)

Opt PICS: Protocol Implementation Compliance statement for v 2.1 specification

Deliverables Ordering information

PGY-RFFE-EX-PD RFFE Protocol Exerciser and Analyzer

- ✓ PGY-RFFE-EX-PD Unit
- ✓ USB3.0 cable
- ✓ PGY-RFFE-EX-PD Software in CD
- ✓ 12V DC adopter
- ✓ Flying lead probe cable with female connector to connect to DUT



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About Prodigy Technovations Pvt Ltd

Prodigy Technovations Pvt Ltd (www.prodigytechno.com) is a leading global technology provider of Protocol Decode, and Physical layer testing solutions on test and measurement equipment. The company's ongoing efforts include successful implementation of innovative and comprehensive protocol decode and physical layer testing solutions that span the serial data, telecommunications, automotive, and defense electronics sectors worldwide.