

PGY-SPMI-EX-PD SPMI Protocol Exerciser & Analyzer



SPMI Protocol Exerciser & Analyzer

SPMI (System Power Management Interface) is a MIPI (Mobile Industry Processor Interface) standard with 2-wire synchronous serial, bi-directional interface that connects the integrated Power Controller (PC) of a System-on-Chip (SoC) processor system with one or more Power Management Integrated Circuits (PMIC) voltage regulation systems.

PGY-SPMI-EX-PD is the leading instrument that enables the design and test engineers to test the SPMI designs for its specifications by configuring PGY-SPMI-EX-ED as master/slave, generating SPMI traffic with error injection capability and decoding SPMI Protocol decode packets.

Features:

- **Support SPMI v 1.0 or 2.0 specifications**
- Ability to configure it as Master or Slave
- **Supports Request Capable Slave (RCS) feature**
- Generate different SPMI Packets
- Error injection such as parity error, ACK/NACK error and Skip SSC error
- Variable SPMI data speeds (32kHz – 26Mhz)
- Simultaneously generate SPMI traffic and Protocol decode of the Bus
- Timing diagram of Protocol decoded bus
- Listing view of Protocol activity
- Error Analysis in Protocol Decode
- Ability to write exerciser script to combine multiple data frame generation at different data speeds
- USB2/3 host computer interface
- **Continuous streaming protocol activity to host system HDD/SSD**
- **API support for automation in Python or C#**
- Flexibility to upgrade to the unit for evolving SPMI Specification
- Optional Protocol Implementation Compliance Statement (**PICS**) support scripts

Product Setup



Comprehensive Protocol Analysis using Multi-View

The screenshot displays the PGY-SPMI-EX-PD software interface with the following sections:

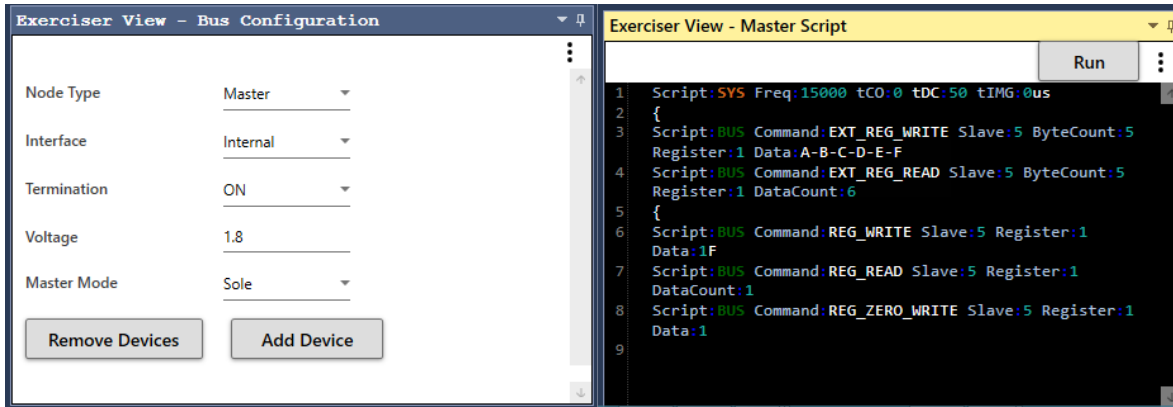
- Setup view:** Shows configuration options like Trace Directory, Trigger Selection (Trigger Type: Auto), and If/Then conditions.
- Plot View:** Displays a timing diagram for SCLK and SDATA signals. A bus activity bar below the plot shows events like 'MPL Primary', 'MPL Secondary', 'SSC Slave=0x06', 'REG_WRITE -0x41', and 'Data=0x01'.
- Exerciser View - Bus Configuration:** Shows settings for Node Type (Master), Interface (Internal), Termination (ON), Voltage (1.8), and Master Mode (Sole).
- Decoded Result:** A table listing protocol transactions with columns for S. No, Time, Slave/MID, Command, Frequency, ByteCount, Reg Address, Data, and Error.

S. No	Time	Slave/MID	Command	Frequency	ByteCount	Reg Address	Data	Error
0	112.292µs	0x6	REG_WRITE	976.57 KHz	-	0x1	Data - 1	Pass
1	160.420µs	0x6	REG_READ	976.57 KHz	-	0x1	Data - 1	Pass
2	207.524µs	0x6	EXT_REG_WRITE	976.57 KHz	0x1	0x2	Data - 2	Pass
3	274.084µs	0x6	EXT_REG_READ	976.57 KHz	0x1	0x2	Data - 2	Pass
4	339.620µs	0x6	EXT_REG_WRITE_LONG	976.57 KHz	0x2	0x12	Data - 3	Pass
5	424.612µs	0x6	EXT_REG_READ_LONG	976.57 KHz	0x2	0x12	Data - 3	Pass
6	508.580µs	0x6	REG_ZERO_WRITE	976.57 KHz	-	0x0	Data - 1	Pass
7	547.492µs	0x5	AUTHENTICATE	976.57 KHz	-	0x0	Data - 8	Pass
8	665.252µs	0x5	DDB_SEL_R	976.57 KHz	-	0x0	Data - 11	Pass
9	795.300µs	0x6	SLEEP	976.57 KHz	-	0x0	Data - 1	Pass
10	834.212µs	0x6	REG_READ	976.57 KHz	-	0x1	Data - 1	Error

Version: 0.8.9

Multidomain View provides the complete view of SPMI Protocol activity in single GUI. User can easily setup the analyzer to generate SPMI traffic using a GUI or script. User can set different trigger conditions from the setup menu to capture Protocol activity at specific event and decode the transition between Master and Slave. The decoded results can be viewed in timing diagram and Protocol listing window with autocorrelation. This comprehensive view of information makes it industry best, offering an easy to use solution to debug the SPMI protocol activity. Continuous streaming protocol activity to host system HDD/SSD ensures seamless roll mode operation without the need to recapture data when DUT/s are set to different states thereby saving test times.

Exerciser:



PGY-SPMI-EX-PD supports SPMI traffic generation using GUI and Script. User can generate simple traffic generation using the GUI to test the DUT. Script based GUI provides flexibility to emulate the complete expected traffic in real world including error injections. In this sample script user can generate SPMI traffic as below.

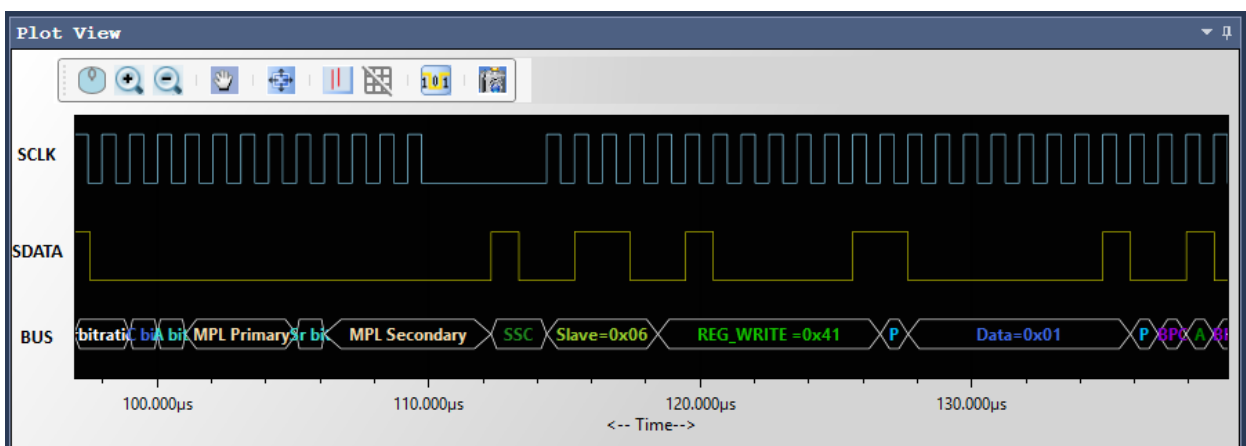
Script line #3: Ext Reg Write to the slave with USID 05

Script line #4: Ext Reg Read to the slave with USID 05

Script line #6: Reg Write to the slave with USID 05

Script line #7: Reg Read to the slave with USID 05

Timing Diagram and Protocol Listing View



Timing view provides the plot of SCL and SDA signals with bus diagram. Overlaying of Protocol bits on the digital timing waveform will help easy debugging of Protocol decoded data. Cursor and Zoom features will make it convenient to analyze Protocol in timing diagram for any timing errors.

Decoded Result									
S.No	Time	Slave/MID	Command	Frequency	ByteCount	Reg Address	Data	Error	
0	112.292µs	0x6	REG_WRITE	976.57 KHz	-	0x1	Data - 1	Pass	
1	160.420µs	0x6	REG_READ	976.57 KHz	-	0x1	Data - 1	Pass	
2	207.524µs	0x6	EXT_REG_WRITE	976.57 KHz	0x1	0x2	Data - 2	Pass	
3	274.084µs	0x6	EXT_REG_READ	976.57 KHz	0x1	0x2	Data - 2	Pass	
4	339.620µs	0x6	EXT_REG_WRITE_LONG	976.57 KHz	0x2	0x12	Data - 3	Pass	
5	424.612µs	0x6	EXT_REG_READ_LONG	976.57 KHz	0x2	0x12	Data - 3	Pass	
6	508.580µs	0x6	REG_ZERO_WRITE	976.57 KHz	-	0x0	Data - 1	Pass	
7	547.492µs	0x5	AUTHENTICATE	976.57 KHz	-	0x0	Data - 8	Pass	
8	665.252µs	0x5	DDB_SL_R	976.57 KHz	-	0x0	Data - 11	Pass	
9	795.300µs	0x6	SLEEP	976.57 KHz	-	0x0		Pass	
10	834.212µs	0x6	REG_READ	976.57 KHz	-	0x1	Data - 1	Error	

Protocol window provides the decoded packet information in each state and all packet details. Selected frame in Protocol listing window will be auto correlated in timing view to view the timing information of the packet.

Powerful Trigger Capabilities

Trigger Selection

Trigger Type **Advanced**

Level Count **2**

Level # 0

If

SSC	Ext_Reg_W	Slave/MID: 5	Byte Count: 1
Register Address: 1		Data	
Then	Action: Nothing	Go to Level: 1	

Else If

SSC	Reg_Write	Slave/MID: 5	
Register Address: 1		Data	
Then	Action: Trigger		

PGY-SPMI-EX-PD supports simple trigger capabilities. Analyzer can trigger on any of the Protocol packets such as Reg Write, SLEEP or WAKE UP. Advanced Trigger provides the flexibility to monitor Multiple trigger conditions and can set multiple state trigger machine. User can initiate a timer and trigger on set timer values.

<i>PGY-SPMI-EX-PD Specification</i>	<i>Features</i>	<i>PGY-SPMI-EX-PD</i>
Exerciser:		
<i>Configurable</i>	<i>1 Master + 2 Slaves</i>	✓
<i>SPMI Traffic Generation</i>	<i>Custom SPMI traffic generation</i>	✓
	<i>Simulate real world network traffic</i>	✓
<i>SCL Frequency</i>	<i>32 kHz to 26 MHz</i>	✓
<i>Voltage Drive Level</i>	<i>1.2V or 1.8V</i>	✓
<i>Command sequence Support</i>	<i>All command sequence is supported except DDB master Read</i>	✓
<i>SCLK Duty Cycle variation</i>	<i>YES. (can be 25%, 50%, 75%)</i>	✓
<i>SCLK & SDATA Delay</i>	<i>Resolution (4ns)</i>	✓
<i>Delay between two messages</i>	<i>YES</i>	✓
<i>Specification</i>	<i>SPMI 1.0 and SPMI 2.0</i>	✓
<i>SPMI network</i>	<i>Sole master and multi master</i>	✓
<i>Error injection</i>	Master - <ul style="list-style-type: none"> <i>Data parity,</i> <i>command parity,</i> <i>address parity</i> <i>Skip SSC (only in Sole master systems)</i> Slave - <ul style="list-style-type: none"> <i>Data parity (NON RCS)</i> 	✓
Protocol Analysis:		
<i>Supports</i>	<i>SPMI protocol decode</i>	✓
<i>Protocol Views</i>	<i>Timing Diagram View</i> <i>Protocol Listing View</i> <i>Bus-Diagram to display Protocol packets with timing diagram plot</i>	✓
<i>Protocol Trigger</i>	<i>Simple (Trigger on user defined SPMI packet after SSC)</i>	✓
<i>Capture Duration</i>	<i>Continuous streaming Protocol Data</i>	✓
<i>Protocol Error Report</i>	<i>Data parity,</i> <i>command parity,</i> <i>address parity</i> <i>ACK/ NACK error</i>	✓
<i>Host Connectivity</i>	<i>USB 3.0 / 2.0 interface</i>	✓

Ordering Information

PGY-SPMI-EX-PD SPMI Protocol Exerciser and Analyzer (Please mention the specification needed)

-Opt **PICS (Protocol Implementation Compliance Statement test scripts)**

(Please Specify version to be supported V1.0/V2.0)

Deliverables for PGY-SPMI-EX-PD

PGY-SPMI-EX-PD Unit

USB3.0 cable

PGY-SPMI-EX-PD Software in CD

12V DC adopter

Flying lead probe cable with female connector to connect to DUT

Contact Information

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About Prodigy Technovations Pvt Ltd

Prodigy Technovations Pvt Ltd (www.prodigytechno.com) is a leading global technology provider of Protocol Decode, and Physical layer testing solutions on test and measurement equipment. The company's ongoing efforts include successful implementation of innovative and comprehensive protocol decode and physical Layer testing solutions that span the serial data, telecommunications, automotive, and defense electronics sectors worldwide.