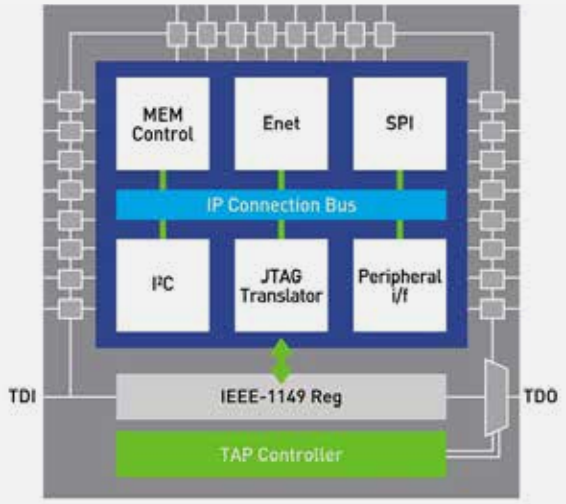
Factsheet

CORECOMMANDER AND JTAG TRANSLATOR FOR FPGAS

Direct access to memory and peripheral controllers in FPGAs for testing, debugging and fast in-system programming.



- Direct access to memory and peripheral (I/O) controllers in an FPGA through its JTAG interface
- Read data from, write data to memory and peripherals without software programming
- At-speed execution of read and write cycles
- Testing and debugging of the connections between an FPGA and memory and peripherals with at-speed bus cycles without software programming
- Easy programming of flash memory without software programming

JTAG Translator is an IP[1] module from JTAG Technologies that provides a JTAG interface bridge to the internal IP connection bus of an FPGA to which peripherals / peripheral controllers are connected. JTAG Translator is operated through a dedicated CoreCommander software module that can be used with JTAGLive and ProVision as well as with all our production packages. CoreCommander provides high-level functions to write data to and read data from memory and I/O addresses without software programming. CoreCommander functions are applied via the JTAG interface. The JTAG Translator IP module can be loaded in the FPGA for test configurations only, or it can be included as permanent standard feature in functional designs.

With JTAG Translator the IP blocks which are already used in a design can be re-used for test or in-system programming purposes. Examples of existing IP blocks are interface controllers for SDR, DDR, Ethernet Mac, USB, UART, I2C, CAN, etc... These are readily available from different IP suppliers such as Altera, Xilinx, OpenCores, etc.. ...

Applications

CoreCommander is used in design debug, manufacturing test and (field) service for applications such as:

- Checking the integrity of the connections between an FPGA and memory or I/O devices by writing data to and reading data back from these devices via the memory and peripheral controllers in the FPGA
- Determining the right settings for the peripheral controller (DDR controller, flash memory controller, I/O controller) in combination with your particular memory or peripheral device. Write settings into controller registers and verify whether proper access to memory or I/O is possible with those settings.
- Programming board (serialnr) specific data such as calibration values, a mac address or a timestamp in memory, or program an entire flash.

Order information
CoreComm FPGA (vendor)
(vendor) = Altera, Xilinx

[1] Functional blocks like memory controllers and other peripheral controllers are often referred to as Intellectual Property (IP) blocks.

Background

While an FPGA generally includes a boundary-scan register allowing tests and in-system programming operations to be performed, engineers can also use the Translator plus CoreCommander, when the architecture allows. Whether the Translator plus CoreCommander or the boundary-scan register is used will depend on preference or performance.

Factsheet

CORECOMMANDER AND JTAG TRANSLATOR FOR FPGAS

Direct access to memory and peripheral controllers in FPGAs for testing, debugging and fast in-system programming.

An FPGA may contain a number of peripheral controllers or peripherals that are connected via an internal IP connection bus. Externally peripherals are connected to the peripheral controllers. Communication with these blocks is via read and write operations on the bus to which they are connected. Different internal busses exist such as: Wishbone, Avalon, AMBA, etc..

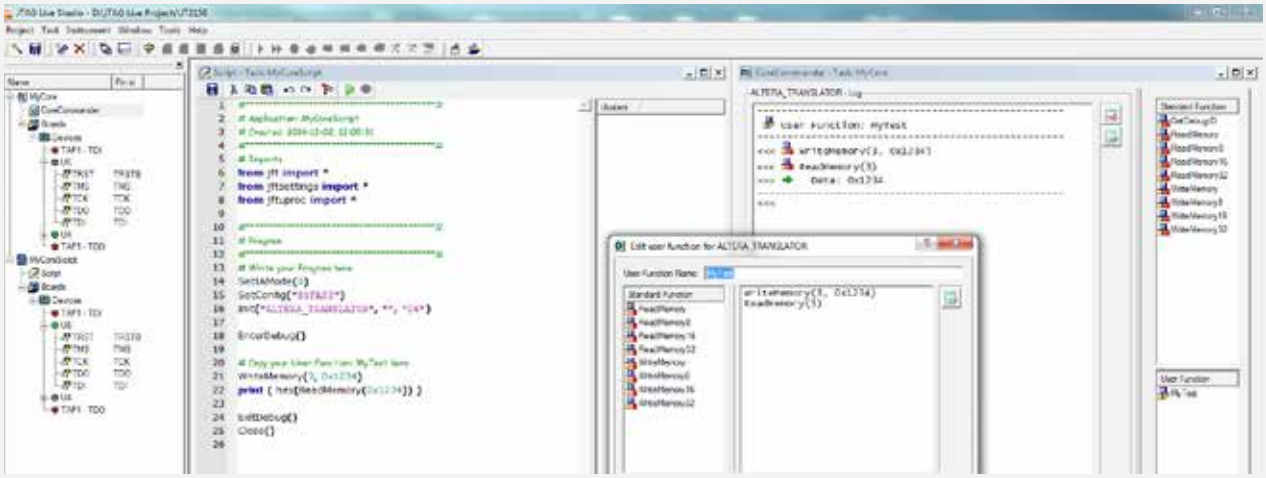
To make this bus accessible via the JTAG interface the JTAG Translator can be added. Now commands to write data to and read data from memory and I/O addresses can be given through the translator. Commands are given to the translator using the CoreCommander.
The testing of memory connections or programming a flash memory using CoreCommander is a simple straightforward sequence of write and read commands.

Usage

CoreCommander can be used as interactive hardware debug tool via its high-level GUI. In this interface register access commands or full memory reads and writes can be selected and executed with a direct view of the results. Sequences of commands can be re-played within the interactive window or exported into a Python editor. The interactive usage is particularly valuable during hardware bring up and debugging in design and (field) service.
For **automated scripts** the functions from CoreCommander can be called directly from programming (scripting) environments such as Python, LabView, LabWindows, Visual basic, C, C++, .NET and TestStand. This is highly valuable to create re-usable tests for specific devices or clusters and for in-system flash programming.

- Generic RTL coded solution for FPGAs provides IP core access via Wishbone, Avalon, AMBA, etc..
- Available for FPGA's from Altera, Xilinx
- Ask your JTAG supplier for the support for your FPGA.

Figure 2



CoreCommander GUI and Python code

Region or Country	Telephone	E-mail
• **Europe or Rest of World**	+31 (0)40 295 0870	info@jtag.nl
• **United Kingdom & Ireland**	+44 (0)1234 831212	sales@jtag.co.uk
• **North America**	Toll free - 877 FOR JTAG Western US - 949 454 9040	info@jtag.com
• **China, Malaysia, Singapore, Thailand, Taiwan**	+86 (021) 5831 1577	info@jtag.com.cn
• **Germany**	+49 (0)971 6991064	germany@jtag.com
• **Finland**	+358 (0)9 4730 2670	finland@jtag.com
• **Sweden**	+46 (0)8 754 6200	sweden@jtag.com

Q1_2015_1001