BG950A-GL&BG951A-GL

Hardware Design

LPWA Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

	Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.
	Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergent help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.
	The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.
	In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

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-	2021-07-07	Lex LI/ Ben JIANG	Creation of the document
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1 Introduction

This document helps you gain a quick insight into BG950A-GL and BG951A-GL modules, their air and hardware interfaces, electrical and mechanical specifications, and other related information, as well. In addition, it includes some reference designs that, coupled with application notes and user guides, facilitate the development and deployment of your LPWA module applications.

NOTE

For conciseness purposes, BG950A-GL and BG951A-GL modules will hereinafter be referred to collectively as "the module/modules" in parts hereof applicable to both modules, and individually as "BG950A-GL" and "BG951A-GL" in parts hereof referring to the differences between them.

1.1. Special Mark

Table 1: Special Mark

Mark	Definition
*	Unless otherwise specified, when an asterisk (*) is used after a function, feature, interface, pin name, AT command, or argument, it indicates that the function, feature, interface, pin, AT command, or argument is under development and currently not supported; and the asterisk (*) after a model indicates that the sample of the model is currently unavailable.

2 Product Overview

The module is an embedded IoT (LTE Cat M1, NB1/NB2*) wireless communication module. It supports data connectivity on LTE HD-FDD network, and features GNSS functionality to meet your specific application demands.

It is an SMD type module that can be engineered into M2M applications, such as smart metering, tracking system, security, wireless POS, and other wearable devices.

The module is an industrial-grade module for industrial and commercial applications only.

Related information and details are listed in the table below.

Table 2: Brief Introduction of the Module

Categories	
Packaging and pins number	LGA; 102 pieces
Dimensions	(23.6 ±0.2) mm × (19.9 ±0.2) mm × (2.2 ±0.2) mm
Weight	Approx. 2.15 g
Wireless technologies	LTE and GNSS
Variants	BG950A-GL, BG951A-GL

2.1. Frequency Bands and Functions

Table 3: Wireless Network Types

Module	Supported Bands	Power Class	GNSS
BG950A-GL	**Cat M1:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/B20/ B25/B26/B27/B28/B66 **Cat NB1/NB2*** [1]**:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B17/B18/B19/ B20/B25/B28/B66	Power Class 3 (23 dBm ± 2.7 dB)	GPS, GLONASS.
BG951A-GL	**Cat M1:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B18/B19/B20/ B25/B26/B27/B28/B66 **Cat NB1/NB2*** [1]**:** LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B17/B18/B19/ B20/B25/B28/B66	Power Class 3 (23 dBm ± 2.7 dB)	GPS, GLONASS, BDS, Galileo, QZSS.

NOTE

The baseband chip of BG950A-GL integrates the GNSS function, whereas the internal baseband chip and GNSS chip are separated on BG951A-GL. Therefore, BG951A-GL supports concurrent operation of LTE and GNSS, whereas BG950A-GL does not.

[1] LTE Cat NB2* is backward compatible with LTE Cat NB1.

2.2. Key Features

Table 4: Key Features

Features	Details
Power Supply	● Supply voltage: 2.2–4.35 V ● Typical supply voltage: 3.3 V
SMS	● Text and PDU mode ● Point-to-point MO and MT ● SMS cell broadcast ● SMS storage: ME by default
(U)SIM Interface	Supports 1.8 V external (U)SIM/eSIM card only
USB Interface	● Compliant with USB 2.0 specifications ● Supports full speed mode only ● Used for AT command communication, data transmission, software debugging and firmware upgrade* ● USB serial driver: - Windows 7/8/8.1/10 - Linux 2.6–5.15
UART Interfaces	**Main UART:** ● Used for AT command communication and data transmission ● Baud rate: 115200 bps by default ● Default frame format: 8N1 (8 data bits, no parity, 1 stop bit) ● Supports RTS and CTS hardware flow control **CLI UART [2]:** ● Used for firmware upgrade, software debugging, log output, GNSS data and NMEA sentence output ● Baud rate: 115200 bps by default ● Default frame format: 8N1 (8 data bits, no parity, 1 stop bit) ● Supports RTS and CTS hardware flow control **Debug UART:** ● Used for RF calibration and log output ● Baud rate: 961200 bps by default ● Default frame format: 8N1 (8 data bits, no parity, 1 stop bit) ● Supports RTS and CTS hardware flow control **GNSS UART:** ● Only BG951A-GL module: used for GNSS data and GNSS NMEA sentence output, and GNSS firmware upgrade

[2] BG951A-GL only supports one CLI UART interface, while BG950A-GL supports two CLI UART interfaces, more precisely, pin 27 (CLI_TXD1) and pin 28 (CLI_RXD1) are connected to pin 95 (CLI_TXD2) and pin 94 (CLI_RXD2) respectively inside the module.

	• Baud rate: 115200 bps by default
Network Indication	Pin NET_STATUS to indicate network connectivity status
AT Commands	• *3GPP TS 27.007* and *3GPP TS 27.005* AT commands • Quectel enhanced AT commands
Antenna Interface	• Main antenna interface (ANT_MAIN), 50 Ω impedance • GNSS antenna interface (ANT_GNSS), 50 Ω impedance
Transmitting Power	Class 3 (23 dBm ±2.7 dB) for LTE HD-FDD bands
LTE Features	• Supports 3GPP Rel-13/Rel-14* • Supports LTE Cat M1, NB1/NB2* • Supports 1.4 MHz RF bandwidth for LTE Cat M1 • Supports 200 kHz RF bandwidth for LTE Cat NB1/NB2* • Rel-13: Cat M1: 300 kbps (DL)/375 kbps (UL) Cat NB1: 27.2 kbps (DL)/62.5 kbps (UL) • Rel-14*: Cat M1: 588 kbps (DL)/1119 kbps (UL) Cat NB2*: 127 kbps (DL)/158 kbps (UL)
Internet Protocol Features	• Supports PPP/TCP/UDP/SSL/MQTT/FTP(S)/HTTP(S)/LwM2M/IPv4/IPv6/ TLS/DTLS/PING/CoAP/NITZ protocols • Supports PAP and CHAP for PPP connections
GNSS Features	• BG950A-GL: GPS, GLONASS • BG951A-GL: GPS, GLONASS, BDS, Galileo, QZSS
Temperature Range	• Operating temperature range [3]: -35 to +75 °C • Extended temperature range [4]: -40 to +85 °C • Storage temperature range: -40 to +90 °C
Firmware Upgrade	• CLI UART interface [2] • USB 2.0 interface* • DFOTA
RoHS	All hardware components are fully compliant with EU RoHS directive.

[3] Within the operating temperature range, the module meets 3GPP specifications.
[4] Within the extended temperature range, the module retains the ability to establish and maintain functions such as SMS and data transmission, without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified 3GPP tolerances. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

2.3. Functional Diagram

The block diagrams and major functional parts of BG950A-GL and BG951A-GL are illustrated in the following figures.

- Power management
- Baseband
- Radio frequency
- Peripheral interfaces

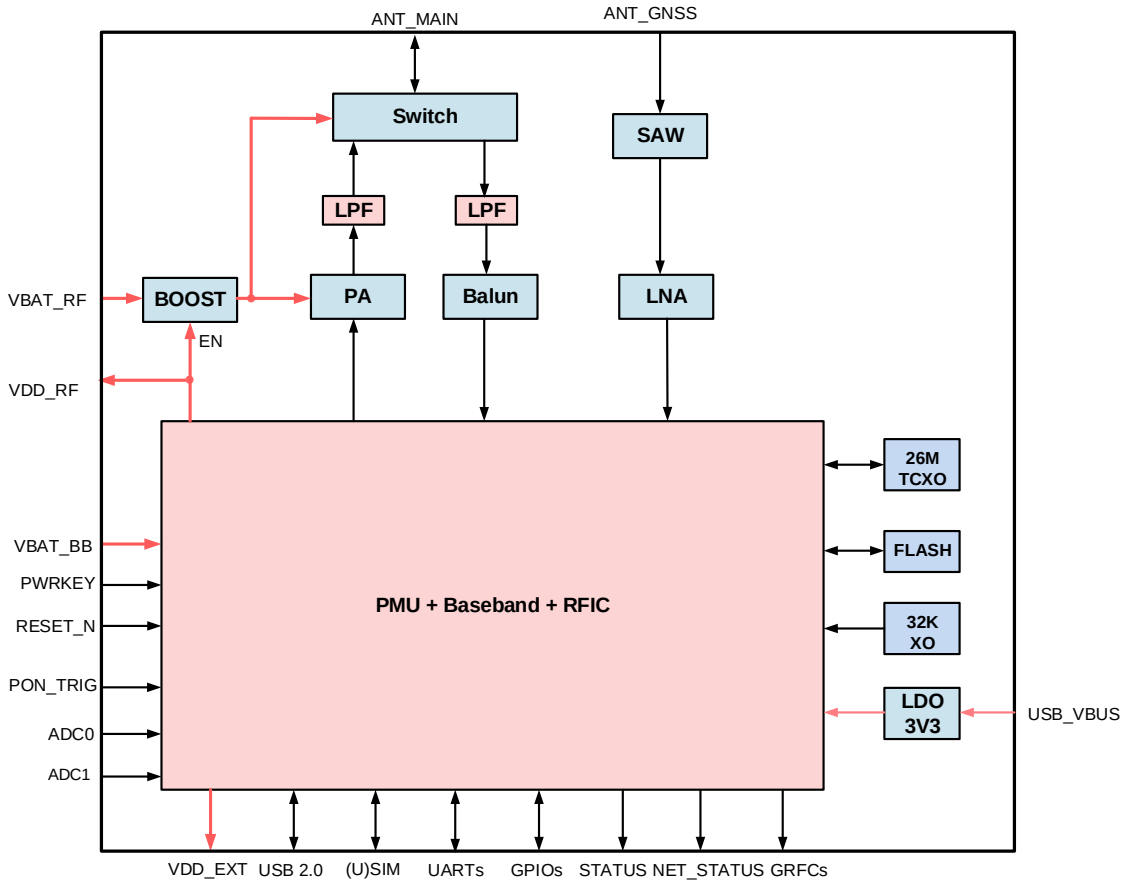


Figure 1: Functional Diagram of BG950A-GL

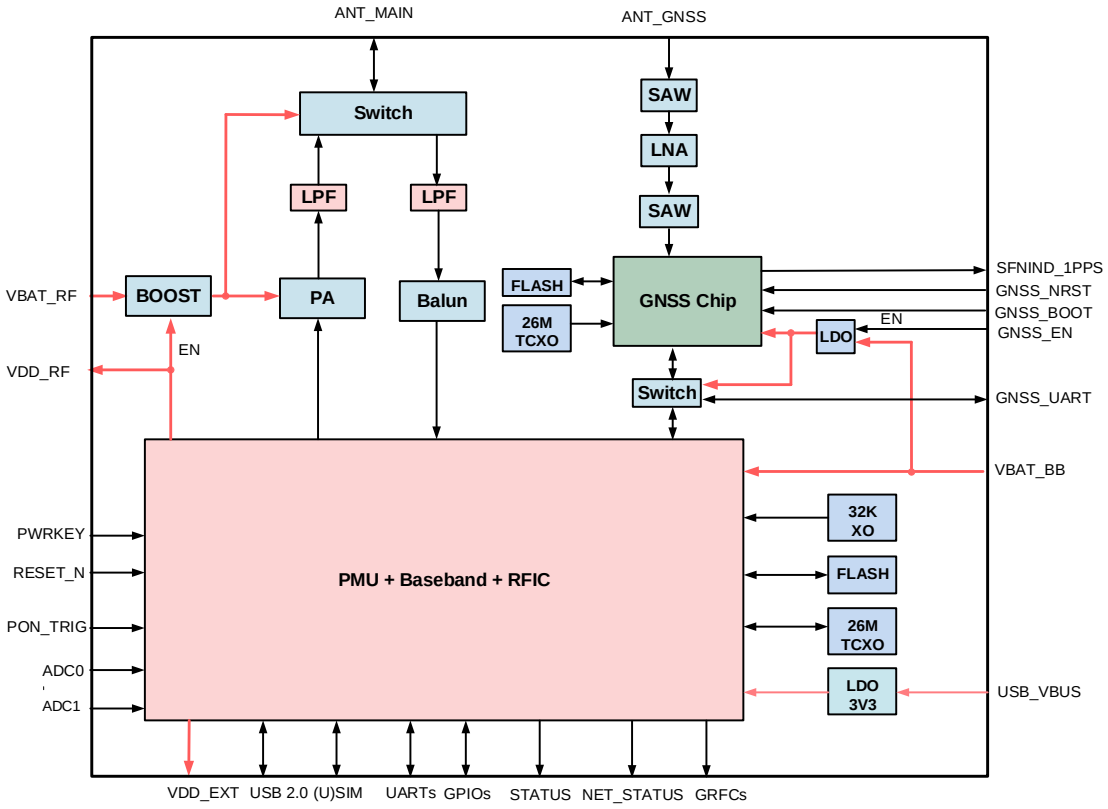


Figure 2: Functional Diagram of BG951A-GL

2.4. Pin Assignment

The following figure illustrates the pin assignment of BG950A-GL.

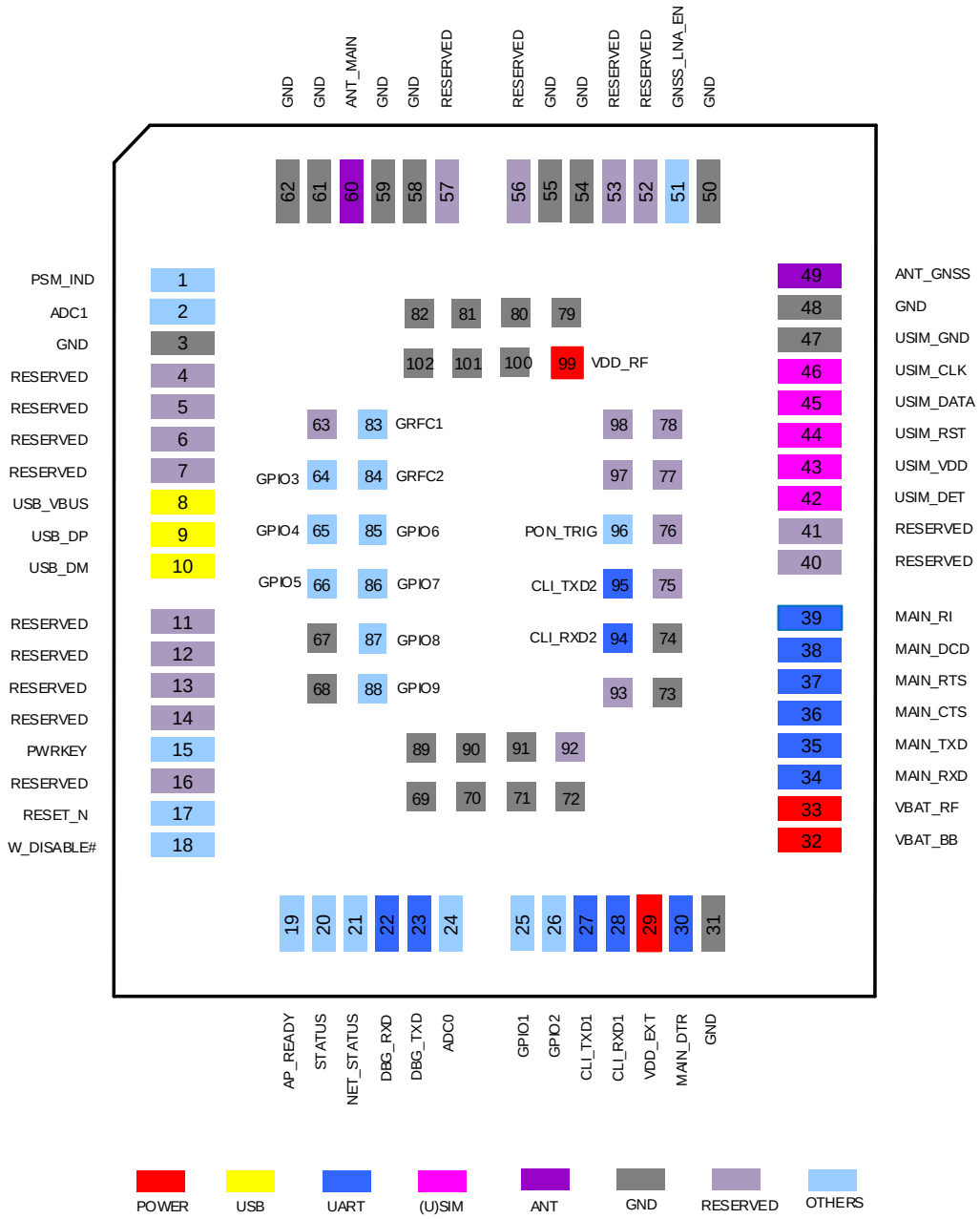


Figure 3: Pin Assignment of BG950A-GL (Top View)

The following figure illustrates the pin assignment of BG951A-GL.

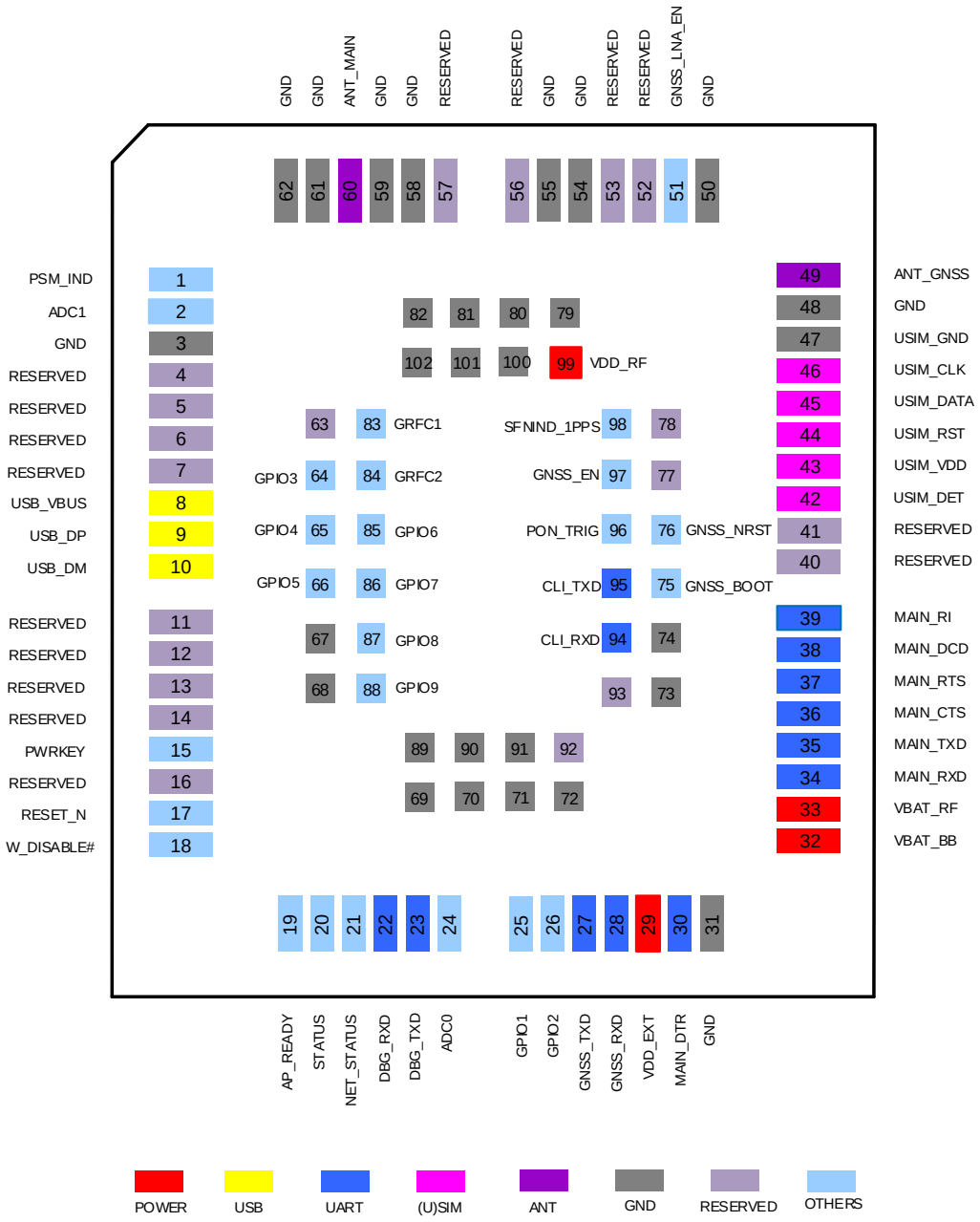


Figure 4: Pin Assignment of BG951A-GL (Top View)

NOTE

1. ADC input voltage must not exceed 1.8 V.
2. Keep all RESERVED pins and unused pins unconnected.
3. GND pins should be connected to ground in the design.
4. Only BG951A-GL supports GNSS_BOOT (pin 75), GNSS_NRST (pin 76), GNSS_EN (pin 97) and

SFNIND_1PPS (pin 98).

5. On BG950A-GL, pin 27 (CLI_TXD1) and pin 28 (CLI_RXD1) are connected to pin 95 (CLI_TXD2) and pin 94 (CLI_RXD2) respectively inside the module.
6. The LNA is integrated inside the module. It is not recommended to use an external LNA. It is strongly recommended to keep GNSS_LNA_EN (pin 51) and VDD_RF (pin 99) unconnected.

2.5. Pin Description

The following table shows the DC characteristics and pin descriptions.

Table 5: I/O Parameters Definition

Type	Description
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
OD	Open Drain
PI	Power Input
PO	Power Output

Table 6: Pin Definition – Pins with Same Functions on BG950A-GL and BG951A-GL

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT_BB	32	PI	Power supply for the module's baseband part	Vmax = 4.35 V Vmin = 2.2 V Vnom = 3.3 V	See NOTE 1.
VBAT_RF	33	PI	Power supply for the module's RF part		See NOTE 1.
VDD_EXT	29	PO	Provide 1.8 V for external circuits	Vnom = 1.8 V $I_O$max = 50 mA	If unused, keep this pin open.

GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102				
Turn On/Off					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PWRKEY	15	DI	Turn on/off the module	V_{IL}max = 0.3 V V_{IH}min = 1.0 V	Internally pulled up with a 470 kΩ resistor.
Reset					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESET_N	17	DI	Reset the module	V_{IL}max = 0.3 V V_{IH}min = 1.3 V	Internally pulled up with a 470 kΩ resistor.
Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PSM_IND	1	DO	Indicate the module's power saving mode	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	1.8 V power domain. If unused, keep these pins open.
STATUS	20	DO	Indicate the module's operation status		
NET_STATUS	21	DO	Indicate the module's network activity status		
USB Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USB_VBUS	8	AI	USB connection detect	Vnom = 5.0 V	Typical 5.0 V
USB_DP	9	AIO	USB differential data (+)	Vmax = 4.1 V Vmin = -0.2 V	Compliant with the standard USB 2.0 specification. Requires differential impedance of 90 Ω.
USB_DM	10	AIO	USB differential data (-)		
(U)SIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_DET	42	DI	(U)SIM card hot-plug detect	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.

USIM_VDD	43	PO	(U)SIM card power supply	Vmax = 1.9 V Vmin = 1.7 V	Only 1.8 V (U)SIM card is supported.
USIM_RST	44	DO	(U)SIM card reset	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	1.8 V power domain.
USIM_DATA	45	DIO	(U)SIM card data	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V V_{OL}max = 0.36 V V_{OH}min = 1.44 V	
USIM_CLK	46	DO	(U)SIM card clock	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	
USIM_GND	47	-	Specified ground for (U)SIM card	-	-
Main UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_DTR	30	DI	Main UART data terminal ready	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep these pins open.
MAIN_RXD	34	DI	Main UART receive		
MAIN_TXD	35	DO	Main UART transmit	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	
MAIN_CTS	36	DO	DTE clear to send signal from DCE (Connect to DTE's CTS)		
MAIN_RTS	37	DI	DTE request to send signal from DCE (Connect to DTE's RTS)	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
MAIN_DCD	38	DO	Main UART data carrier detect	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	
MAIN_RI	39	DO	Main UART ring indication		
Debug UART Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	22	DI	Debug UART receive	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep these pins open.
DBG_TXD	23	DO	Debug UART transmit	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	

Antenna Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_MAIN	60	AIO	Main antenna interface	-	50 Ω impedance
ANT_GNSS	49	AI	GNSS antenna interface		50 Ω impedance. If unused, keep this pin open.
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	25	DIO	General-purpose input/output	V_{OL}max = 0.36 V V_{OH}min = 1.44 V V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep these pins open.
GPIO2	26	DIO			
GPIO3	64	DIO			
GPIO4	65	DIO			
GPIO5	66	DIO			
GPIO6	85	DIO			
GPIO7	86	DIO			
GPIO8	87	DIO			
GPIO9	88	DIO			
ADC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	24	AI	General-purpose ADC interface	0–1.8 V	If unused, keep these pins open.
ADC1	2	AI	General-purpose ADC interface	0–1.8 V	
Other Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
W_DISABLE#	18	DI	Airplane mode control	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. Pulled up by default. When this pin is at a low level, the

					module can enter airplane mode. If unused, keep this pin open.
AP_READY*	19	DI	Application processor sleep state detect	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep this pin open.
PON_TRIG	96	DI	Used for main UART function control and for entering/exiting e-I-DRX, PSM, sleep or power off modes	V_{IL}min = -0.2 V V_{IL}max = 0.3 V V_{IH}min = 1 V V_{IH}max = 1.98 V	1.8 V power domain. Pulled down by default.
GRFC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	83	DO	Generic RF controller	V_{OL}max = 0.36 V V_{OH}min = 1.44 V V_{OH}max = 2.0 V	1.8 V power domain. If unused, keep these pins open.
GRFC2	84	DO	Generic RF controller		
External GNSS LNA Interface [5]					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GNSS_LNA_EN	51	DO	External GNSS LNA enable	V_{OL}max = 0.38 V V_{OH}min = 1.36 V	1.8 V power domain. If unused, keep this pin open.
VDD_RF	99	PO	Can be used for external GNSS LNA power supply	Vnom = 1.9 V $I_O$max = 50 mA	If unused, keep this pin open.
RESERVED Pins					
Pin Name	**Pin No.**				**Comment**
RESERVED	4–7, 11–14, 16, 40, 41, 52, 53, 56, 57, 63, 77, 78, 92, 93				Keep these pins open.

[5] The LNA is integrated inside the module. It is not recommended to use an external LNA. It is strongly recommended to keep GNSS_LNA_EN (pin 51) and VDD_RF (pin 99) unconnected.

Table 7: Pin Definition – Pins with Different Functions on BG950A-GL and BG951A-GL

Pin No.	BG950A-GL		BG951A-GL		I/O	DC Characteristics	Comment
	Pin Name	Pin Description	Pin Name	Pin Description			
94	CLI_RXD2	CLI UART2 receive	CLI_RXD	CLI UART receive	DI	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep these pins open.
95	CLI_TXD2	CLI UART2 transmit	CLI_TXD	CLI UART transmit	DO	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	
27	CLI_TXD1	CLI UART1 transmit	GNSS_TXD	GNSS UART transmit	DO	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	1.8 V power domain. If unused, keep these pins open.
28	CLI_RXD1	CLI UART1 receive	GNSS_RXD	GNSS UART receive	DI	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	
75	RESERVED	Reserved	GNSS_BOOT	Force the GNSS chip of the module into emergency download mode	DI	V_{IL}min = -0.2 V V_{IL}max = 0.54 V V_{IH}min = 1.26 V V_{IH}max = 2.0 V	1.8 V power domain. If unused, keep these pins open.
76	RESERVED	Reserved	GNSS_NRST	Reset the GNSS chip; Active high	DI		
97	RESERVED	Reserved	GNSS_EN	Enable internal GNSS chip	DI		
98	RESERVED	Reserved	SFNIND_1PPS	One pulse per second	DO	V_{OL}max = 0.36 V V_{OH}min = 1.44 V	Synchronized at the rising edge. Pulse width: 100 ms. If unused, keep it open.

NOTE

1. When the module starts up normally, to ensure full functionality, the minimum supply voltage should be higher than 2.2 V. For every VBAT transition/re-insertion from 0 V, VBAT slew rate < 25 mV/μs. To ensure normal module startup, pulling down PWRKEY to turn on the module after VBAT remains stable for 100 ms.
2. After entering PSM or power off mode, it is prohibited to provide any external voltage to the module's I/O ports that are not defined as a wake-up source.
3. Keep all RESERVED pins and unused pins unconnected.

2.6. EVB Kit

To help you develop applications with the module, Quectel supplies an evaluation board (UMTS&LTE EVB) with accessories to control or test the module. For more details, see ***document [1]***.

3 Operating Characteristics

3.1. Operating Modes

The table below outlines operating modes of the module.

Table 8: Operating Mode Overview

Mode	Details	
Normal Operation	Idle	The module remains registered on the network and is ready to send and receive data. In this mode, the software is active.
	Connected	The module is connected to the network. Its current consumption varies with the network setting and data transfer rate.
Extended Idle Mode DRX (e-I-DRX)	The module and network may negotiate over non-access stratum signaling the use of e-I-DRX for reducing power consumption while being available for mobile terminated data and/or network originated procedures within a certain delay dependent on the DRX cycle value.	
Airplane Mode	**AT+CFUN=4** or W_DISABLE# pin can set the module to airplane mode where the RF function is invalid.	
Minimum Functionality	**AT+CFUN=0** can set the module to minimum functionality without removing the power supply. In this mode, both RF function and (U)SIM card are invalid.	
Sleep Mode	The module retains the ability to receive paging messages, SMS and TCP/UDP data from the network normally. In this mode, the current consumption is reduced to a low level.	
Power OFF Mode	The module's power supply is shut down by its power management unit. The software is inactive, the serial interfaces are inaccessible, while the operating voltage of VBAT_BB/RF is still maintained.	
Power Saving Mode (PSM)	PSM is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections. The current consumption is minimized.	
Recovery Mode	The module can burn firmware with an empty serial flash, or recover from firmware malfunction. For more details, see ***Chapter 3.6***.	

NOTE

In e-I-DRX mode, it is recommended to use the main UART interface for data communication, as the use of USB interface will increase power consumption.

3.2. Airplane Mode

When the module enters airplane mode, the RF function will be disabled, and all AT commands correlative with RF function will be inaccessible. This mode can be set as follows:

Hardware:

W_DISABLE# is pulled up by default. Driving it low will make the module enter airplane mode.

Software:

AT+CFUN=<fun> provides functionality level choices by setting **<fun>** to 0, 1 or 4.

- **AT+CFUN=0:** Minimum functionality. Both RF and (U)SIM functions are disabled.
- **AT+CFUN=1:** Full functionality (default).
- **AT+CFUN=4:** Airplane mode (RF function is disabled).

NOTE

1. Airplane mode control via W_DISABLE# is disabled in firmware by default. It can be enabled with **AT+QCFG="airplanecontrol"**. For more details of the command, see ***document [2].***
2. On BG950A-GL, the execution of **AT+CFUN** will affect the GNSS function. Since the module does not support concurrent operation of LTE and GNSS, the GNSS function can be used when **<fun>**=0 or 4, but cannot be used when **<fun>**=1.
3. On BG951A-GL, the execution of **AT+CFUN** will not affect the GNSS function.

3.3. Power Saving Mode (PSM)

The module minimizes its power consumption by entering PSM. The mode is similar to power-off, but the module remains registered on the network and there is no need to re-attach or re-establish PDN connections. Therefore, in PSM the module cannot immediately respond to user requests.

When the module wants to use PSM, it shall request an Active Time value during every Attach and TAU procedure. If the network supports PSM use, it will allocate an Active Time value to the module to confirm

PSM use. If the module wants to change the Active Time value, the module consequently requests the value it wants in the TAU procedure.

If PSM is supported by the network, then it can be enabled via **AT+QPSMS**. In this case, driving PON_TRIG low will set the module to PSM.

Any of the following methods can wake up the module from PSM:

- Driving PON_TRIG high and keeping it high, will wake up the module from PSM.
- When the TAU timer expires, the module wakes up from PSM automatically. In this case, the main UART interface is inaccessible until PON_TRIG is pulled up.
- Driving PWRKEY low to wake up the module from PSM. In this case, the main UART interface is inaccessible until PON_TRIG is pulled up.

NOTE

1. PON_TRIG is pulled down by default.
2. PON_TRIG must be pulled up after executing any PSM wake-up event, otherwise the main UART will be inaccessible. In any case, the main UART interface is inaccessible until PON_TRIG is pulled up.
3. See ***document [3]*** for details about **AT+QPSMS**.

3.4. Extended Idle Mode DRX (e-I-DRX)

The module (UE) and the network may negotiate over non-access stratum signalling the use of e-I-DRX for reducing its power consumption, while being available for mobile terminating data and/or network originated procedures within a certain delay dependent on the DRX cycle value.

Applications that want to use e-I-DRX need to consider specific handling of mobile terminating services or data transfers, and in particular, they need to consider the delay tolerance of mobile terminated data.

In order to negotiate the use of e-I-DRX, the UE requests e-I-DRX parameters during attach procedure and RAU/TAU procedure. The EPC may reject or accept the UE request for enabling e-I-DRX. In case the EPC accepts e-I-DRX, the EPC based on operator policies and, if available, the e-I-DRX cycle length value in the subscription data from the HSS, may also provide different values of the e-I-DRX parameters than what was requested by the UE. If the EPC accepts the use of e-I-DRX, the UE applies e-I-DRX based on the received e-I-DRX parameters. If the UE does not receive e-I-DRX parameters in the relevant accept message because the EPC rejected its request or because the request was received by EPC not supporting e-I-DRX, the UE shall apply its regular discontinuous reception.

3.4.1. e-I-DRX Sleep Mode

If e-I-DRX is supported by the network, perform the steps below in sequence to make the module enter e-I-DRX sleep mode, in which case the main UART interface is inaccessible.

1. Send **AT+QPSMS=0** to disable the use of PSM.
2. Send **AT+CEDRXS=1** to enable the use of e-I-DRX.
3. Send **AT+QSCLK=2** to enable sleep mode.
4. Drive MAIN_DTR high.
5. Drive PON_TRIG low.

To make the module exit e-I-DRX sleep mode, perform the steps below in sequence.

1. Drive PON_TRIG high.
2. Drive MAIN_DTR low.
3. Send **AT+QSCLK=0** to disable sleep mode.
4. Send **AT+CEDRXS=0** to disable the use of e-I-DRX mode.
5. Send **AT+QPSMS=0** to enable the use of PSM (optional).

3.4.2. e-I-DRX Idle Mode

If e-I-DRX is supported by the network, just send **AT+CEDRXS=1** to make the module enter e-I-DRX idle mode, or send **AT+CEDRXS=0** to make the module exit e-I-DRX idle mode.

NOTE

See ***document [3]*** for details about the above AT commands.

3.5. Sleep Mode

The module can reduce its power consumption during the sleep mode. Power saving procedures and sleep mode are outlined in the following sub-sections.

3.5.1. UART Application Scenario

If the host communicates with the module via the main UART interface, perform the steps below in sequence to make the module enter the sleep mode, in which case the main UART interface is not accessible.

1. Send **AT+CFUN=0** to set the module to minimum functionality [6].
2. Drive MAIN_DTR low.
3. Execute **AT+QSCLK=2** to enable sleep mode.
4. Drive MAIN_DTR high.
5. Drive PON_TRIG low.

When the module is in sleep mode, perform the steps below in sequence to make the module exit sleep mode.

1. Drive PON_TRIG high.
2. Drive MAIN_DTR low.
3. Execute **AT+QSCLK=0** to disable sleep mode.
4. Send **AT+CFUN=1** to set the module to full functionality [6].
5. Drive MAIN_DTR high.

The figure illustrates the connection between the module and the host.

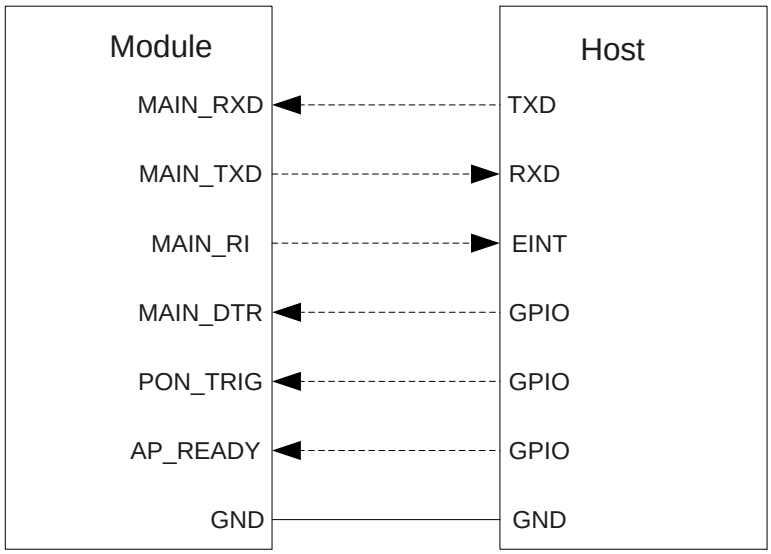


Figure 5: Sleep Mode Application via UART Interface

- When the module has a URC to report, MAIN_RI will wake up the host. See ***Chapter 4.5.4*** for details about MAIN_RI behavior.
- After the module is turned on, MAIN_DTR is internally pulled up by default.
- AP_READY will detect the sleep state of the host (it can be configured to detect high or low voltage level). See **AT+QCFG="apready"** in ***document [2]*** for details.

[6] After setting the module to minimum functionality with **AT+CFUN=0**, you can test the lowest power consumption of the module after the module enters sleep mode. If you need to keep the RF function on after the module enters sleep mode, there is no need to send any **AT+CFUN** command.

3.6. Recovery Mode

The module features the recovery mode for firmware upgrade in emergency cases. Recovery mode can force the baseband chip of the module to upgrade firmware via the CLI UART interface(s) [7].

The following preconditions can set the module to recovery mode.

1. Short-circuit CLI_TXD & CLI_RXD on BG951A-GL, or CLI_TXD2 & CLI_RXD2 on BG950A-GL.
2. Drive PWRKEY low to turn on the module. In this case the module will enter recovery mode.
3. After the module enters recovery mode, disconnect CLI_TXD & CLI_RXD, or CLI_TXD2 & CLI_RXD2.
4. Upgrade firmware via the CLI UART interface(s) [7].

NOTE

1. In recovery mode, pin 25 functions as CLI_RTS and pin 26 functions as CLI_CTS, while in other modes they are GPIO pins.
2. Since the baud rate of the serial port required to download firmware to the baseband chip is 3 Mbps, the flow control pins of the CLI serial port need to be reserved. Otherwise, you can only download with a 921600 baud rate, which is very slow. It is recommended to reserve the test points of the CLI UART interface, including pin 25, pin 26, pin 94 and pin 95, and keep pin 94 close to pin 95.
3. Ensure that VBAT remains stable for at least 100 ms before pulling down PWRKEY.

3.7. Power Supply

3.7.1. Power Supply Pins

The module has two VBAT pins for connection with an external power supply.

- One VBAT_RF pin for RF part.
- One VBAT_BB pin for baseband part.

Table 9: Power Supply Pin Definition

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT_BB	32	Power supply for the module's baseband part	2.2	3.3	4.35	V

[7] On BG950A-GL, it is recommended to use CLI UART2 for firmware upgrade in recovery mode. CLI UART1 is not recommended to be used in this case.

VBAT_RF	33	Power supply for the module's RF part	2.2	3.3	4.35	V
GND	3, 31, 48, 50, 54, 55, 58, 59, 61, 62, 67–74, 79–82, 89–91, 100–102		-	-	-	-

NOTE

For every VBAT transition/re-insertion from 0 V, VBAT slew rate < 25 mV/μs. After the module starts up normally, in order to ensure full functionality, the minimum supply voltage should be higher than 2.2 V.

3.7.2. Voltage Stability Requirements

The power supply range of the module is from 2.2 V to 4.35 V. Make sure that the input voltage never drops below 2.2 V.

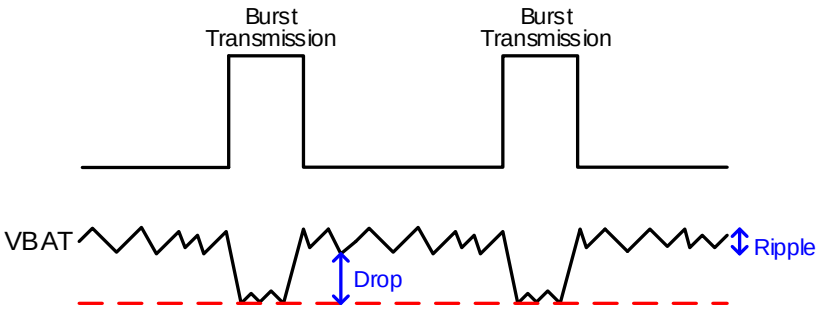


Figure 6: Power Supply Limits During Burst Transmission

To decrease voltage drop, one bypass capacitor of about 100 μF with low ESR and one multi-layer ceramic chip (MLCC) capacitor array for its ultra-low ESR should be used for VBAT_BB/RF. It is recommended to use three ceramic capacitors for composing the MLCC array (100 nF, 33 pF, 10 pF), and place these capacitors close to VBAT pins. The main power supply from an external application must be a single voltage source that can supply power along two star-structured sub paths. The width of VBAT_BB or VBAT_RF trace should be at least 1 mm. In principle, the longer the VBAT trace is, the wider it should be.

In addition, to ensure power supply stability, it is necessary to add two high-power TVS components near VBAT_BB and VBAT_RF. The reference circuit of the power supply is shown below.

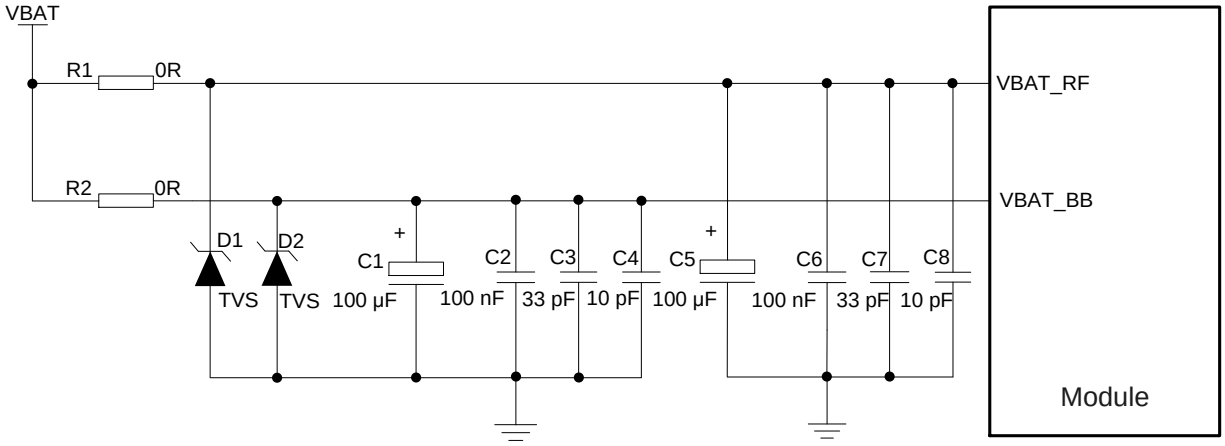


Figure 7: Star Structure of Power Supply

Power design for a module is critical to its performance. The power supply of the module should be able to provide a sufficient current of at least 0.8 A, so it is recommended to select a DC-DC converter chip or an LDO chip with ultra-low leakage current and current output of at least 1.0 A for the power supply design.

3.7.3. Power Supply Monitoring

AT+CBC can be used to monitor the VBAT_BB voltage value. For more details, see ***document [3]***.

3.8. Turn On

3.8.1. Turn On with PWRKEY

Table 10: PWRKEY Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
PWRKEY	15	DI	Turn on/off the module	Internally pulled up with a 470 kΩ resistor.

When the module is in power off mode, driving PWRKEY low for 500–1000 ms and then releasing it will turn on the module. It is recommended to use an open drain/collector driver to control PWRKEY.

A simple reference design is illustrated in the following figure.

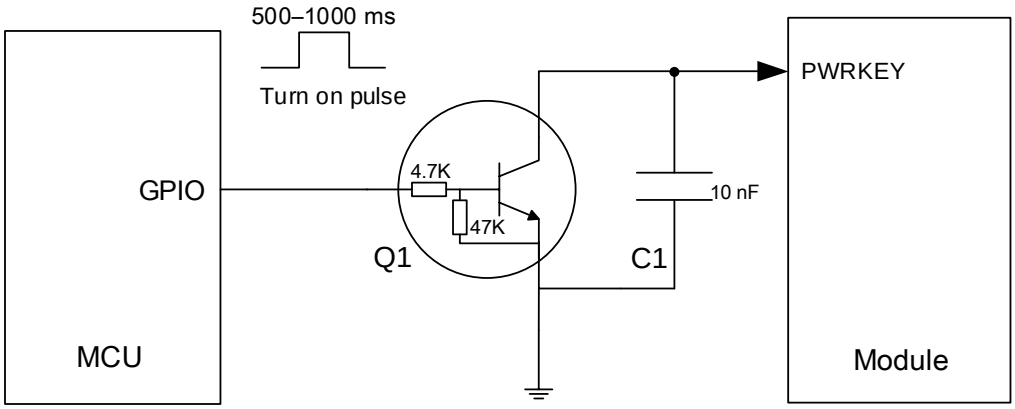


Figure 8: Turn On Module With a Driving Circuit

Another way to control PWRKEY is with a button. Pressing the button may result in a discharge of static electricity from a finger. Therefore, it is vital to place a TVS component near the button for ESD protection.

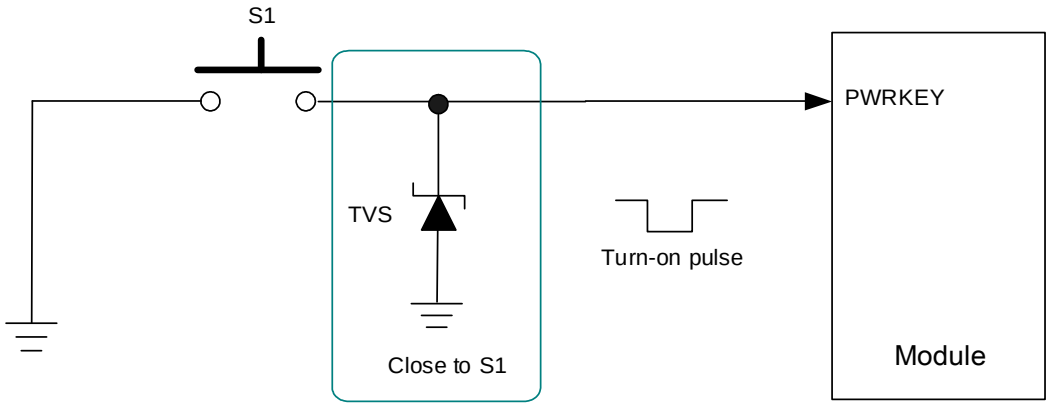


Figure 9: Turn On Module With a Button

Drive PON_TRIG high and then drive PWRKEY low after VBAT is stable for 100–200 ms, the module will be turned on immediately. The power-up timing is shown below.

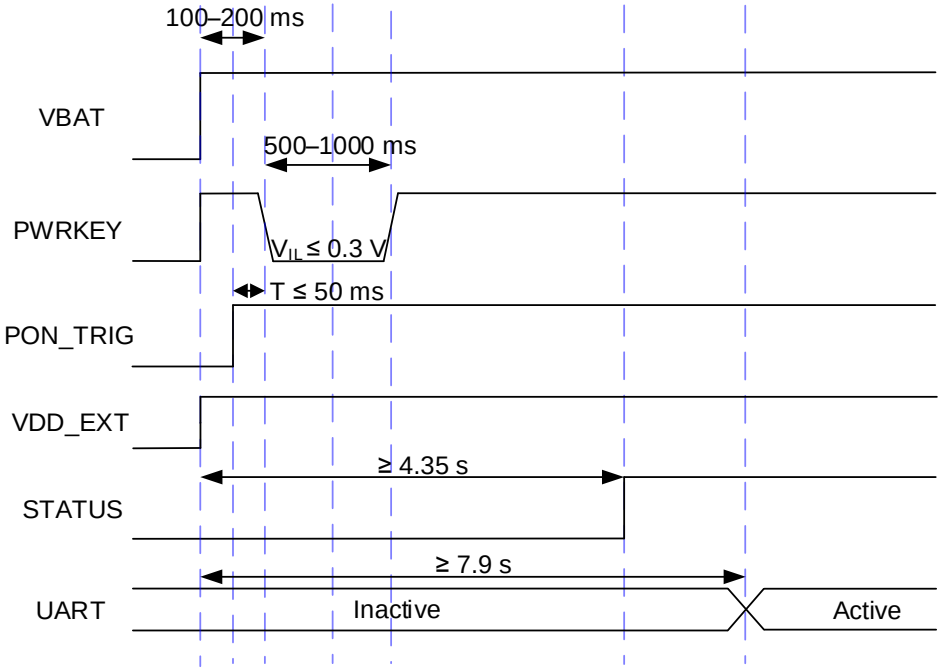


Figure 10: Power-up Timing (After VBAT is Stable for 100–200 ms)

NOTE

1. Ensure that VBAT is stable for 100–200 ms before pulling down PWRKEY.
2. Before you turn on the module by driving PWRKEY low for 500–1000 ms, drive PON_TRIG high, otherwise, the main UART interface will be inaccessible.

Drive PON_TRIG high and then drive PWRKEY low after VBAT is stable for more than 250 ms, the module will be turned on immediately. The power-up timing is shown below.

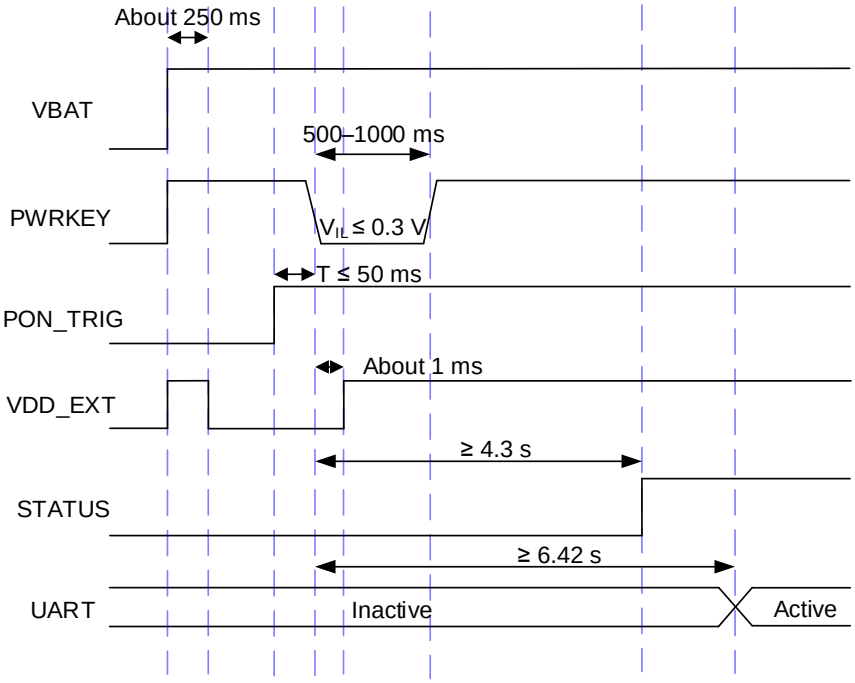


Figure 11: Power-up Timing (After VBAT is Stable for more than 250 ms)

NOTE

1. After VBAT is powered on, it will take about 250 ms for the module to load the internal program.
2. Before the module is turned on by driving PWRKEY low for 500–1000 ms, drive PON_TRIG high, otherwise, the main UART interface will be inaccessible.

After the module is turned off with the PWRKEY and PON_TRIG solution (see ***Chapter 3.9.1***) or the AT command and PON_TRIG solution (see ***Chapter 3.9.2***), VBAT will keep powered on all the time until the main power supply is disconnected. In this case, driving PON_TRIG high and then driving PWRKEY low will restart the module, and the restart timing is shown below.

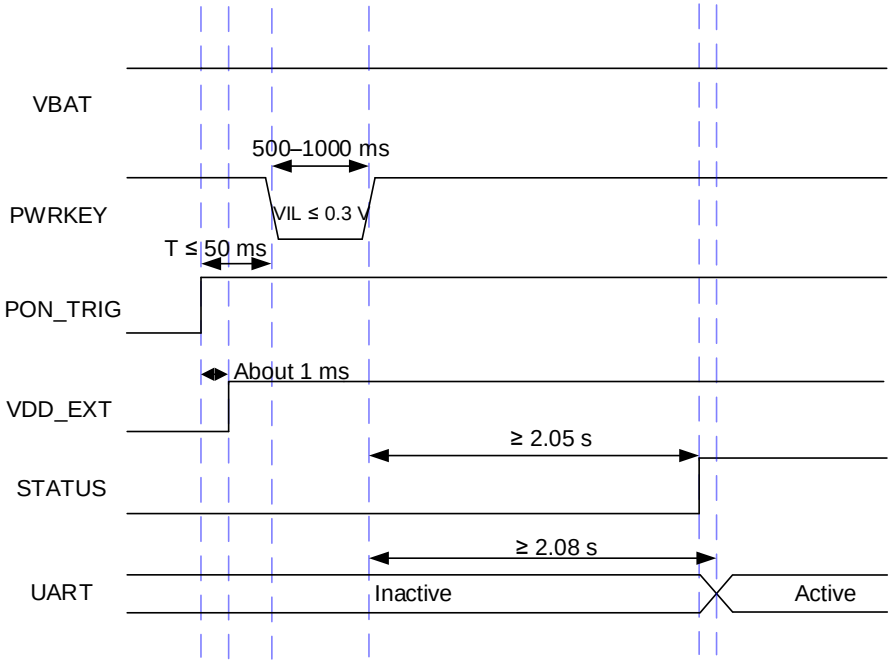


Figure 12: Restart Timing

3.9. Turn Off

After the module is turned off or enters PSM, do not pull up any I/O pin lest it cause additional power consumption and possibly damage pins on the module.

Either of the following methods can be used to turn off the module normally:

- Turn off the module via PWRKEY and PON_TRIG.
- Turn off the module via **AT+QPOWD** and PON_TRIG**.**

3.9.1. Turn Off with PWRKEY and PON_TRIG

When the module is powered on, drive PWRKEY low for 650–1500 ms before releasing it, and then pull down PON_TRIG within 200 ms, after which the module will execute the power-down procedure.

The power-down timing is illustrated in the following figure.

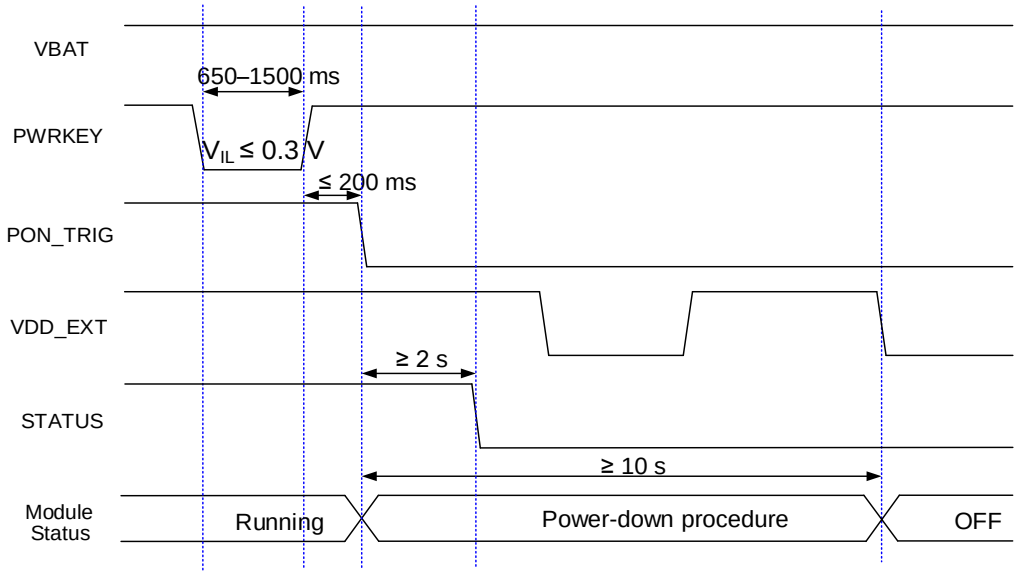


Figure 13: Power-down Timing (PWRKEY & PON_TRIG)

3.9.2. Turn Off with AT Command and PON_TRIG

Similar to PWRKEY, the module can be turned off safely with **AT+QPOWD**. After **AT+QPOWD** is sent, pull down PON_TRIG within 200 ms, and the module will execute the power-down procedure.

See ***document [3]*** for details about **AT+QPOWD**.

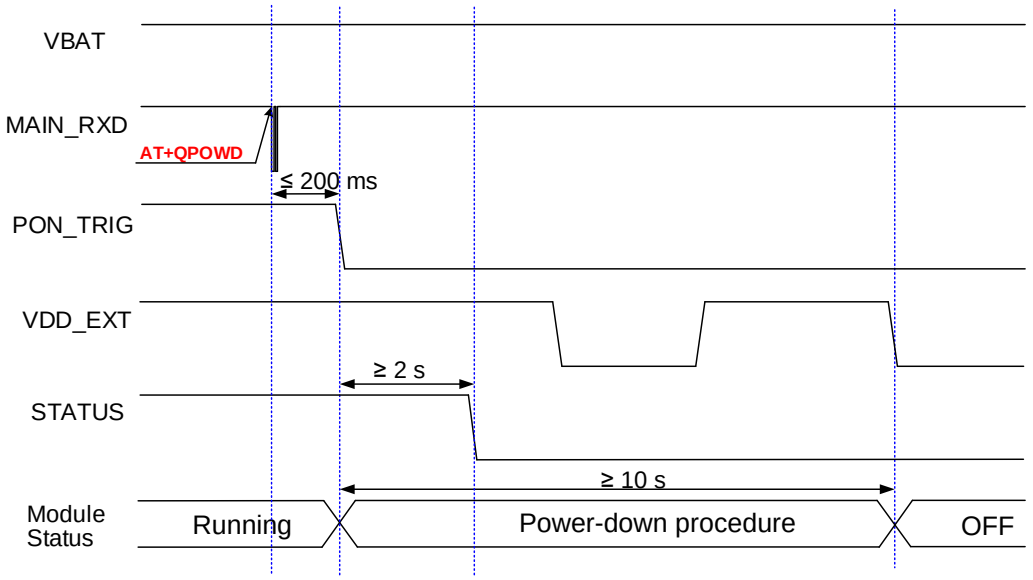


Figure 14: Power-down Timing (AT Command & PON_TRIG)

NOTE

1. To avoid internal flash data damage, do not switch off the power supply while the module is working normally. The power supply can be cut off only after the module is shut down with PWRKEY & PON_TRIG or AT command & PON_TRIG.
2. When turning off the module with AT command, keep PWRKEY at a high level after executing the power-off command. Otherwise, the module will be turned on again after turn-off.

3.10. Reset

The module can be reset by driving RESET_N low for at least 100 ms and then releasing it. The RESET_N signal is sensitive to interference, so it is recommended to route the trace as short as possible and surround it with ground.

Table 11: RESET_N Pin Definition

Pin Name	Pin No.	I/O	Description
RESET_N	17	DI	Reset the module. Internally pulled up with a 470 kΩ resistor.

The recommended circuit is similar to the PWRKEY control circuit. An open drain/collector driver or a button can be used to control RESET_N.

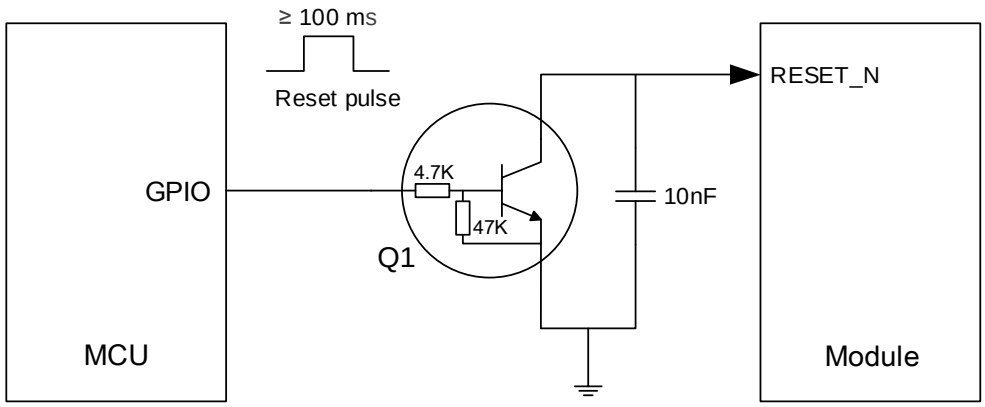


Figure 15: Reference Circuit of RESET_N with a Driving Circuit

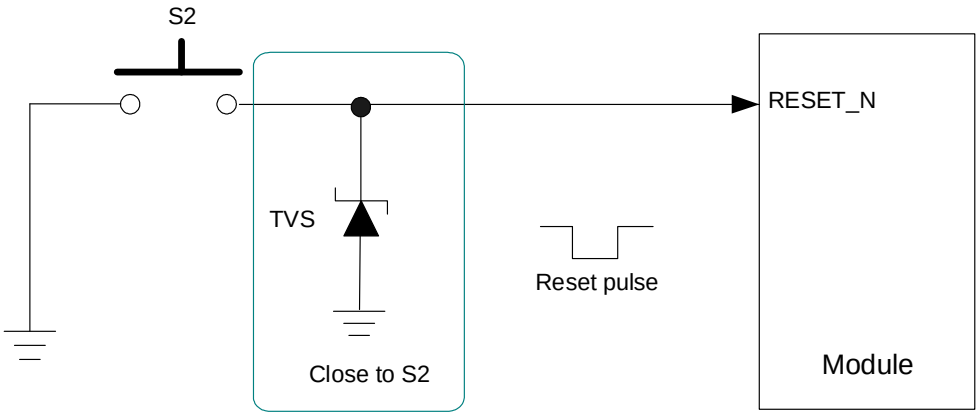


Figure 16: Reference Circuit of RESET_N with a Button

The reset timing is illustrated in the following figure.

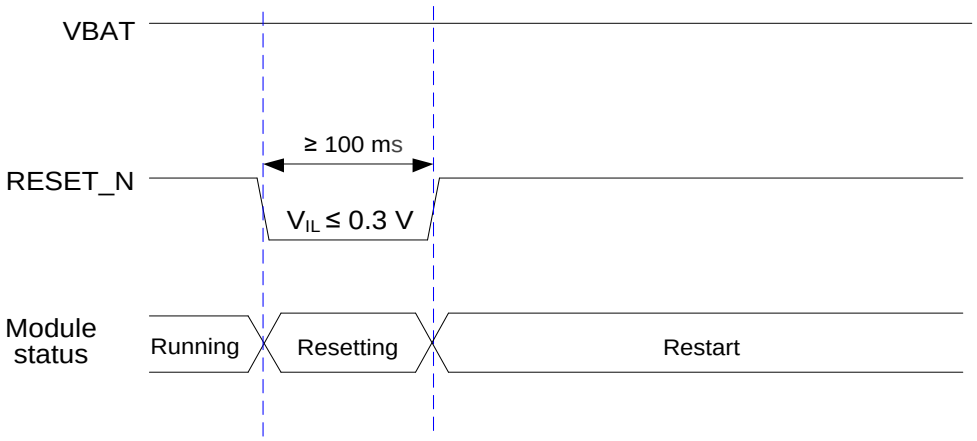


Figure 17: Reset Timing

NOTE

1. Ensure that there is no large capacitance on RESET_N pin.
2. Because PWRKEY and RESET traces are sensitive signal traces, it's necessary to surround the traces with ground on that layer and with ground planes above and below, and keep their traces away from each other, so as to reduce interference.

3.11. PON_TRIG

The module provides one PON_TRIG pin. Drive PON_TRIG high and keep it high to wake up the module

from PSM. PON_TRIG is pulled down by default.

Table 12: Pin Definition of PON_TRIG

Pin Name	Pin No.	I/O	Description	Comment
PON_TRIG	96	DI	Used for main UART function control and for entering/exiting e-I-DRX, PSM, sleep or power off mode.	1.8 V power domain. Pulled down by default.

PON_TRIG has the following functions:

- Makes the module enter or exit e-I-DRX, PSM, sleep or power off mode.
- Enables/disables the main UART interface communication function.
- Turns on/off the module.

PON_TRIG must be designed to allow for external control. A reference circuit is shown in the following figure.

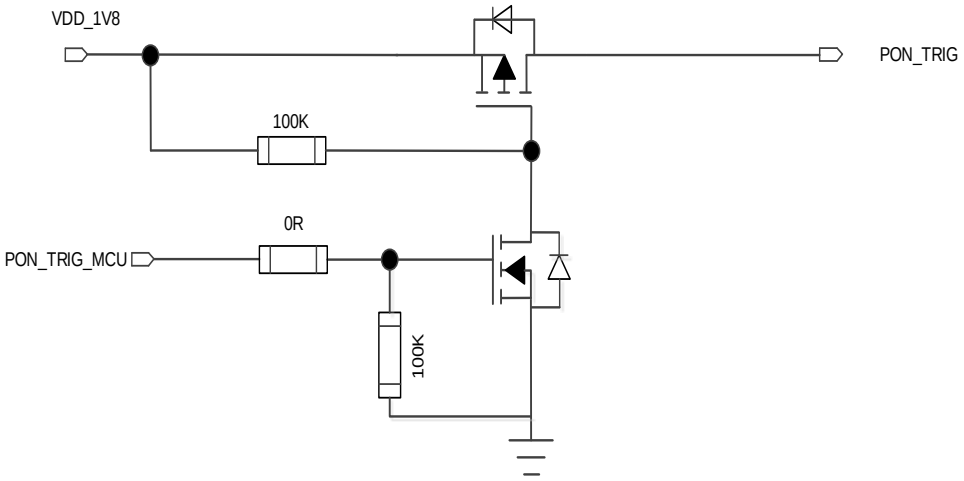


Figure 18: PON_TRIG Reference Circuit 1

In addition, a voltage divider circuit can be used to control PON_RIG. The voltage domain of the external host and the voltage divider resistor should be selected with care. A voltage divider circuit in the 3.3 V host voltage domain is shown in the following figure.

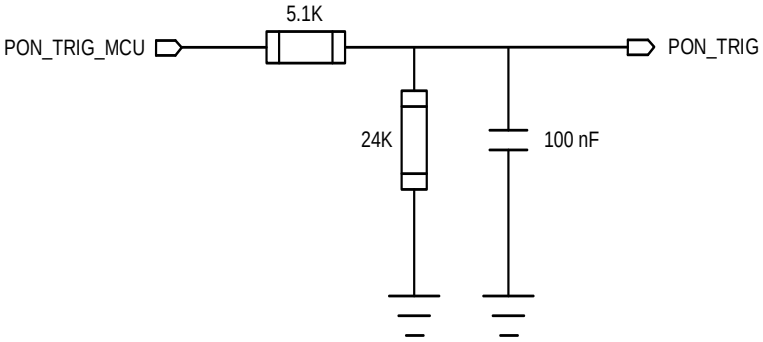


Figure 19: PON_TRIG Reference Circuit 2

NOTE

1. VDD_1V8 is provided by an external LDO.
2. If the host's voltage domain is not 3.3 V, the value of the voltage divider resistors should be tested according to your actual application.
3. Inside the module, PON_TRIG is connected in series with a diode and connected in parallel with a 10 kΩ pull-down resistor to the ground. Therefore, the actual voltage divider value needs to be measured.

The following is a brief description of PON_TRIG use.

- PON_TRIG is pulled down by default. Before the module is turned on, PON_TRIG must be pulled up. Otherwise, the main UART interface will be inaccessible.
- When the module is powered on, pull down PON_TRIG within 200 ms after sending **AT+QPOWED** or driving PWRKEY low, after which the module will execute the power-down procedure. For more details, see ***Chapter 3.9***.
- After sending **AT+QPSMS** to enable PSM, driving PON_TRIG low will set the module to PSM. Drive PON_TRIG high and keep it high, the module will wake up from PSM. In this case, PON_TRIG must remain high, otherwise the module will re-enter PSM.
- Pull down PON_TRIG and keep it low in e-I-DRX, PSM, sleep or power off mode. In other cases, pull up PON_TRIG and keep it high to make sure the main UART is accessible. For details about PON_TRIG use in e-I-DRX and sleep modes, see ***Chapter 3.4*** and ***Chapter 3.5*** respectively.

4 Application Interfaces

4.1. (U)SIM Interface

The module supports 1.8 V (U)SIM card only. The circuitry of (U)SIM interfaces meet ETSI and IMT-2000 requirements.

Table 13: (U)SIM Interface Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
USIM_DET	42	DI	(U)SIM card hot-plug detect	1.8 V power domain. If unused, keep this pin open.
USIM_VDD	43	PO	(U)SIM card power supply	Only 1.8 V (U)SIM card is supported.
USIM_RST	44	DO	(U)SIM card reset	1.8 V power domain.
USIM_DATA	45	DIO	(U)SIM card data	
USIM_CLK	46	DO	(U)SIM card clock	
USIM_GND	47	-	Specified ground for (U)SIM card	-

The module supports (U)SIM card hot-plug via USIM_DET, and both high-level and low-level detections are supported. The function is disabled by default. See **AT+QSIMDET** in ***document [3]*** for more details.

The following figure illustrates a reference design of (U)SIM interface with an 8-pin (U)SIM card connector.

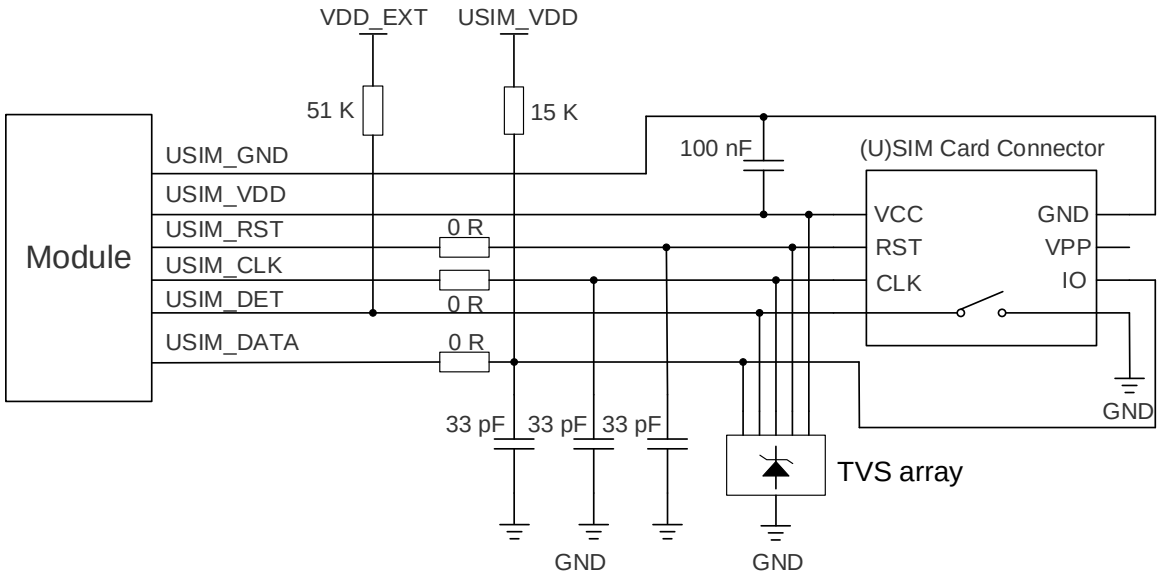


Figure 20: Reference Circuit of (U)SIM Interface with an 8-Pin (U)SIM Card Connector

If (U)SIM card detection function is not needed, keep USIM_DET unconnected. A reference circuit for (U)SIM interface with a 6-pin (U)SIM card connector is illustrated in the following figure.

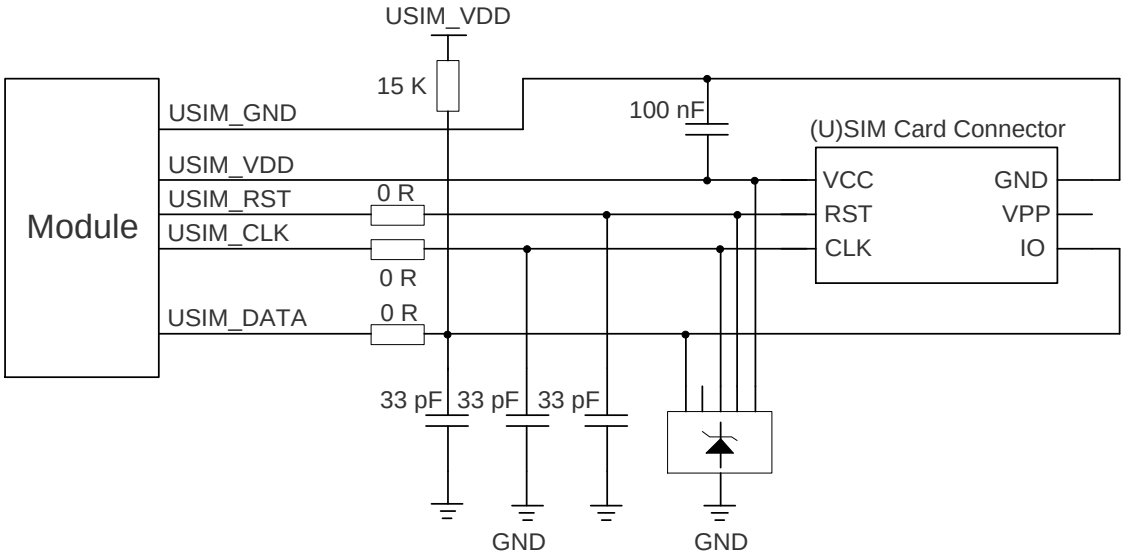


Figure 21: Reference Circuit of (U)SIM Interface with a 6-Pin (U)SIM Card Connector

To enhance the reliability and availability of the (U)SIM card in applications, follow the criteria below in the (U)SIM circuit design:

- Place the (U)SIM card connector as close as possible to the module with a trace shorter than 200 mm.
- Keep (U)SIM card signals away from RF and VBAT traces.

- Ensure a short and wide ground trace between the module and the (U)SIM card connector. Keep the ground and USIM_VDD traces at least 0.5 mm wide to maintain the same electric potential. Make sure the bypass capacitor between USIM_VDD and USIM_GND is less than 1 μF, and place it as close to the (U)SIM card connector as possible. If the system ground plane is complete, USIM_GND can be directly connected to the system ground.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep their traces away from each other and shield them with ground. USIM_RST should also be shielded with ground.
- To offer good ESD protection, it is recommended to add a TVS diode array with parasitic capacitance not exceeding 15 pF. It is recommended to reserve 0 Ω series resistors for the (U)SIM signals of the module to facilitate debugging. The 33 pF capacitors are used for filtering interference of EGSM900. Note that the (U)SIM peripheral circuit should be close to the (U)SIM card connector.
- The pull-up resistor on USIM_DATA trace can improve anti-jamming capability, and should be placed close to the (U)SIM card connector.

4.2. USB Interface

The module features one integrated USB (Universal Serial Bus) interface that complies with the USB 2.0 specification and supports full speed mode only. This USB interface is used for AT command communication, data transmission, software debugging and firmware upgrade*.

The USB interface pin definition is presented in the following table.

Table 14: USB Interface Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
USB_VBUS	8	AI	USB connection detect	Typ. 5.0 V
USB_DP	9	AIO	USB differential data (+)	Compliant with the USB 2.0 standard specification. Requires differential impedance of 90 Ω.
USB_DM	10	AIO	USB differential data (-)	

It is recommended to reserve test points for debugging and firmware upgrading* in your designs.

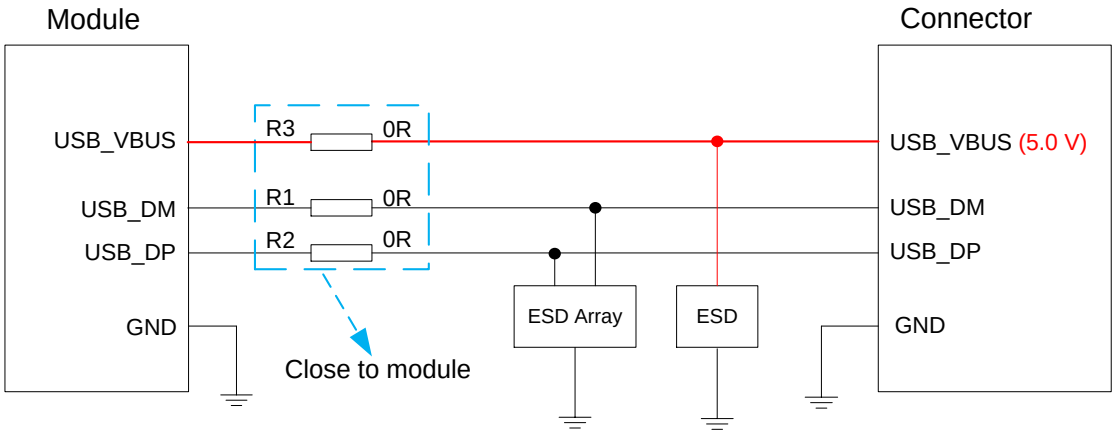


Figure 22: Reference Circuit of USB Application

To ensure USB data signal integrity, if possible, reserve a 0 Ω resistor on USB_DP and USB_DM traces, respectively. Resistors R1 and R2 should be placed close to the module and to each other. The extra trace stubs must be as short as possible.

To meet USB 2.0 specification, comply with the following principles in USB interface designing.

- It is important to route the USB signal traces as a differential pair with ground. The impedance of the USB differential trace is 90 Ω.
- Do not route signal traces under crystals, oscillators, magnetic devices, and RF signal traces. It is important to route the USB differential traces in inner layers of the PCB, and surround the traces with ground on that layer and with ground planes above and below.
- Junction capacitance of the ESD protection device might influence USB data traces, so pay attention to device selection. Typically, the stray capacitance should be less than 2 pF.
- Keep the ESD protection devices as close to the USB connector as possible.
- If possible, reserve a 0 Ω resistor on USB_DP and USB_DM traces, respectively.

For more details about the USB specifications, visit http://www.usb.org/home.

NOTE

1. After the module is turned off or enters PSM, do not pull up any USB interface pin lest it cause additional power consumption and potentially damage pins on the module.
2. When using the UMTS&LTE EVB board to test the USB interface function of the module, please refer to ***document [7]***.

4.3. UART Interfaces

BG950A-GL module provides four UART interfaces: one main UART interface, one debug UART interface and two CLI UART interfaces. BG951A-GL module provides four UART interfaces: one main UART, one debug UART, one CLI UART and one GNSS UART interface.

- **Main UART:**
  It supports 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 and 3000000 bps baud rates. The default baud rate is 115200 bps. It is used for AT command communication and data transmission, and supports RTS and CTS hardware flow control. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit).

- **Debug UART:**
  It supports 921600 bps baud rate by default, and is used for RF calibration and log output, and supports RTS and CTS hardware flow control. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit).

- **CLI UART [8]:**
  It supports 9600, 19200, 38400, 57600, 115200, 230400, 460800, 921600 and 3000000 bps baud rates. The default baud rate is 115200 bps. It is used for firmware upgrade, software debugging, log output, GNSS data and NMEA sentence output, and supports RTS and CTS hardware flow control. The default frame format is 8N1 (8 data bits, no parity, 1 stop bit).

- **GNSS UART (Only Supported by BG951A-GL):**
  The GNSS UART interface supports 115200 bps baud rate by default, and it is used for GNSS data, GNSS NMEA sentence output and GNSS firmware upgrade.

The following tables show the pin definition of four UART interfaces.

Table 15: Main UART Interface Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
MAIN_DTR	30	DI	Main UART data terminal ready	1.8 V power domain. If unused, keep these pins open.
MAIN_RXD	34	DI	Main UART reception	
MAIN_TXD	35	DO	Main UART transmission	
MAIN_CTS	36	DO	DTE clear to send signal from DCE (Connect to DTE's CTS)	

[8] BG951A-GL only supports one CLI UART interface, while BG950A-GL supports two CLI UART interfaces, more precisely, pin 27 (CLI_TXD1) and pin 28 (CLI_RXD1) are connected to pin 95 (CLI_TXD2) and pin 94 (CLI_RXD2) respectively inside the module.

MAIN_RTS	37	DI	DTE request to send signal from DCE (Connect to DTE's RTS)
MAIN_DCD	38	DO	Main UART data carrier detection
MAIN_RI	39	DO	Main UART ring indication

Table 16: Debug UART Interface Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
DBG_TXD	23	DO	Debug UART transmission	1.8 V power domain. If unused, keep them open.
DBG_RXD	22	DI	Debug UART reception	

Table 17: BG950A-GL CLI UART Interface Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
CLI_TXD2	95	DO	CLI UART2 transmission	1.8 V power domain. If unused, keep them open.
CLI_RXD2	94	DI	CLI UART2 reception	
CLI_TXD1	27	DO	CLI UART1 transmission	1.8 V power domain. If unused, keep them open.
CLI_RXD1	28	DI	CLI UART1 reception	

Table 18: BG951A-GL CLI UART Interface Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
CLI_TXD	95	DO	CLI UART transmission	1.8 V power domain. If unused, keep them open.
CLI_RXD	94	DI	CLI UART reception	

Table 19: BG951A-GL GNSS UART Interface Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
GNSS_TXD	27	DO	GNSS UART transmission	1.8 V power domain. If unused, keep them open.
GNSS_RXD	28	DI	GNSS UART reception	

NOTE

AT+IPR can be used to set the baud rate of the main UART interface, and **AT+IFC** can be used to enable/disable the hardware flow control (the function is disabled by default). See ***document [3]*** for more details about these AT commands.

The module features 1.8 V UART interfaces. A level-shifting circuit should be used if your application has a 3.3 V UART interface. It is recommended to use a level-shifting chip without internal pull-up. The voltage-level translator TXB0108PWR manufactured by Texas Instruments is recommended.

The following figure shows a reference design of the main UART interface:

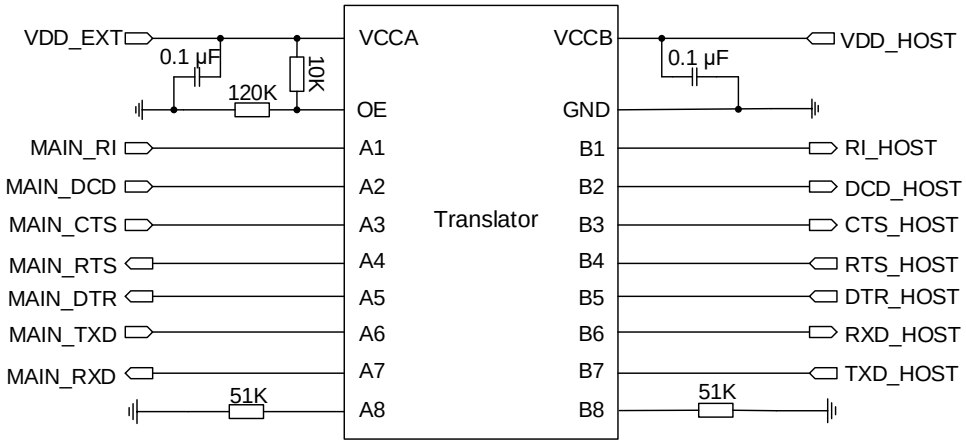


Figure 23: Main UART Reference Design (Translator Chip)

Visit http://www.ti.com for more information.

Another example with a transistor circuit is shown below. For the design of circuits shown in dotted lines, see that of circuits in solid lines, but pay attention to the direction of connection.

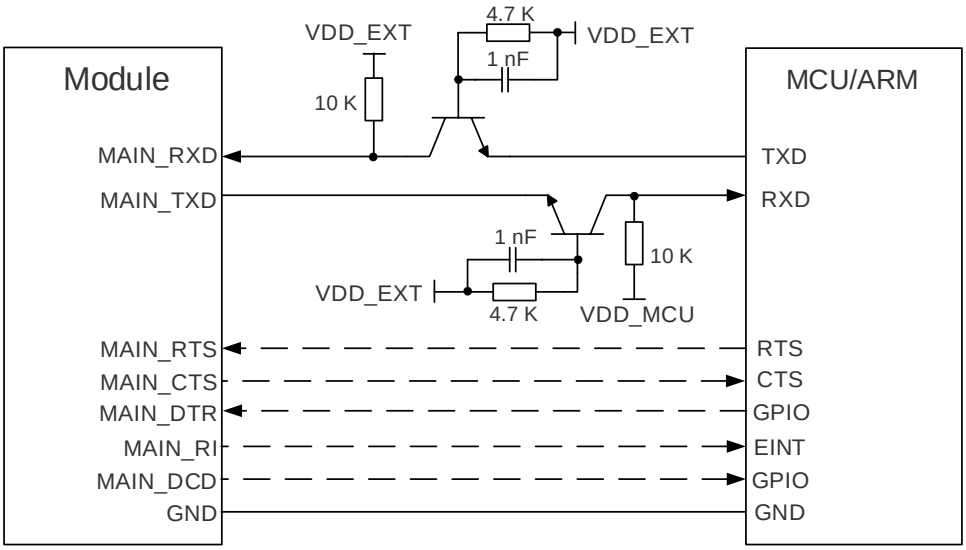


Figure 24: Main UART Reference Design (Transistor Circuit)

NOTE

1. Transistor circuit solution is not suitable for applications with high baud rates exceeding 460 kbps.
2. The main UART interface should be disconnected in PSM and power off modes lest it cause additional power consumption and potentially damage pins on the module.
3. It is recommended to use a level-shifting chip without internal pull-up, such as TXB0108PWR, for level shifting.
4. Please note that the module's CTS is connected to the host's CTS, and the module's RTS is connected to the host's RTS.

4.4. ADC Interfaces

The module provides two ADC (Analog-to-Digital Converter) interfaces. To improve the accuracy of ADC voltage values, the ADC traces should be surrounded with ground.

Table 20: Pin Definition of ADC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
ADC0	24	AI	General-purpose ADC interface	Voltage range: 0–1.8 V
ADC1	2	AI	General-purpose ADC interface	

The voltage value on ADC pins can be read via **AT+QADC=<port>**:

- **AT+QADC=0:** read the voltage value on ADC0.
- **AT+QADC=1:** read the voltage value on ADC1.

For more details about the AT command, see ***document [3]***.

The resolution of the ADC interfaces is up to 12 bits. The following table describes the characteristic of the ADC interfaces.

Table 21: Characteristics of ADC Interfaces

Name	Min.	Typ.	Max.	Unit
Voltage Range	0	-	1.8	V
Resolution	6	-	12	bit

NOTE

1. ADC input voltage must not exceed 1.8 V.
2. It is prohibited to supply any voltage to the ADC pin when VBAT is removed.
3. It is recommended to use a resistor divider circuit for ADC application, and the divider's resistor accuracy should be no less than 1 %.
4. After the module is turned off or enters PSM, do not pull up any pin of ADC interfaces lest it cause additional power consumption and potentially damage pins on the module.

4.5. Indication Signals

4.5.1. PSM Status Indication

Table 22: PSM_IND Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
PSM_IND	1	DO	Indicate the module's power saving mode	1.8 V power domain. If unused, keep this pin open.

When PSM is enabled, the function of PSM_IND will be activated after the module is rebooted. When PSM_IND is at a high level, the module is in a normal operation mode. When it is at a low level, the module is in PSM.

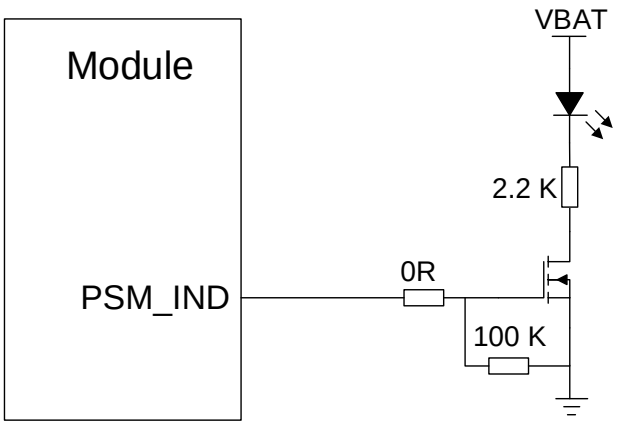


Figure 25: Reference Circuit of PSM Status Indication

4.5.2. Network Status Indication

Table 23: Pin Definition of NET_STATUS

Pin Name	Pin No.	I/O	Description	Comment
NET_STATUS	21	DO	Indicate the module's network activity status	1.8 V power domain. If unused, keep this pin open.

The network indication pin can be used to drive network status indication LEDs. The module features one network indication pin: NET_STATUS. The pin definition and logic level changes in different network status are outlined in the following table.

Table 24: Working State of Network Connection Status Indication

Pin Name	Status	Description
NET_STATUS	Flicker slowly (200 ms High/1800 ms Low)	Network searching
	Flicker slowly (1800 ms High/200 ms Low)	Idle
	Flicker quickly (125 ms High/125 ms Low)	Data transfer is ongoing

A reference circuit is shown in the following figure.

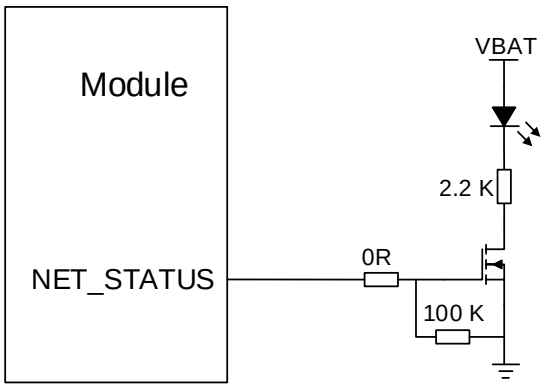


Figure 26: Reference Circuit of Network Status Indication

4.5.3. STATUS

The STATUS pin is an open-drain output for indicating the module's operation status. It will output a high level once the module is powered on successfully.

Table 25: STATUS Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
STATUS	20	DO	Indicate the module's operation status	1.8 V power domain

A reference circuit is shown below.

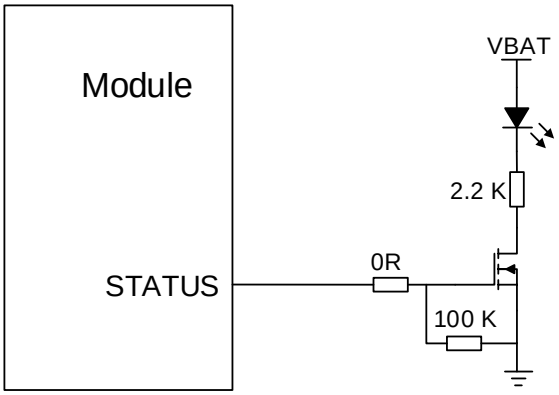


Figure 27: Reference Circuit of STATUS

4.5.4. MAIN_RI

AT+QCFG= "risignaltype","physical" can be used to configure MAIN_RI behavior. No matter on which port a URC is presented, the URC will trigger the behavior of MAIN_RI.

Table 26: MAIN_RI Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
MAIN_RI	39	DO	Main UART ring indication	1.8 V power domain. If unused, keep this pin open.

The default MAIN_RI behaviors can be configured flexibly with **AT+QCFG="urc/ri/ring"**. See ***document [2]*** for details. The default behavior of the MAIN_RI is shown below.

Table 27: MAIN_RI Default Behaviors

State	Response
Idle	MAIN_RI remains at a high level.
URC	MAIN_RI outputs a 120 ms low pulse when a new URC is returned.

NOTE

A URC can be outputted from the main UART interface (default), the debug UART or EMUX ports by configuring URC indication option with **AT+QURCCFG**. See ***document [3]*** for details about **AT+QURCCFG**.

4.6. GRFC Interfaces

The module has two generic RF control interfaces for the control of external antenna tuners.

Table 28: GRFC Interface Pin Definitions

Pin Name	Pin No.	I/O	Description	Comment
GRFC1	83	DO	Generic RF controller	1.8 V power domain. If unused, keep them open.
GRFC2	84	DO	Generic RF controller	

Table 29: GRFC Interface Truth Table

GRFC1 Level	GRFC2 Level	Frequency Range (MHz)
Low	Low	880–2200
Low	High	791–879.9
High	Low	698–790.9

4.7. GPIO Interface

The module has nine general-purpose input and output (GPIO) interfaces. **AT+QCFG="gpio"** can be used to configure the status of GPIO pins. For more details about the AT command, see ***document [2].***

Table 30: GPIO Interface Pin Definitions

Pin Name	Pin No.	I/O	Description	Comment
GPIO1	25	DIO	General-purpose input/output	1.8 V power domain.
GPIO2	26	DIO	General-purpose input/output	
GPIO3	64	DIO	General-purpose input/output	
GPIO4	65	DIO	General-purpose input/output	
GPIO5	66	DIO	General-purpose input/output	
GPIO6	85	DIO	General-purpose input/output	
GPIO7	86	DIO	General-purpose input/output	
GPIO8	87	DIO	General-purpose input/output	
GPIO9	88	DIO	General-purpose input/output	

4.8. GNSS Control and Indication Interfaces

On BG951A-GL module, the GNSS chip is independent of the baseband chip, therefore the module supports the following additional GNSS control and indication pins compared with BG950A-GL.

Table 31: Pin Definition of GNSS Control and Indication Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GNSS_BOOT	75	DI	Force the GNSS chip of the module into emergency download mode	1.8 V power domain. If unused, keep these pins open.
GNSS_NRST	76	DI	Reset the GNSS chip; Active high	
GNSS_EN	97	DI	Enable internal GNSS chip	
SFNIND_1PPS	98	DO	One pulse per second	Synchronized with the NMEA sentences output time at the rising edge. Pulse width: 100 ms. If unused, keep it open.

GNSS_EN is used to enable the LDO that powers the GNSS chip internally. In addition, this LDO can be enabled via the GPIO pins of the internal baseband chip. Pulling up GNSS_EN will power on the GNSS chip. After the module is turned on, the external host can send **AT+QGPS=1** to the GNSS chip via the GNSS UART interface to enable the GNSS function, and then the GNSS chip will output the NEMA sentences from the GNSS UART interface.

GNSS_BOOT is used to upgrade the firmware of the GNSS chip. First, pull up GNSS_BOOT, and then pull up GNSS_EN to supply power for the GNSS chip. After the module is turned on, the GNSS chip will enter the boot mode. At this time, you can use the QFlash tool to update the GNSS firmware. After the update is completed, pull down GNSS_BOOT.

1PPS output via SFNIND_1PPS is disabled by default. You can enable it with **AT+QGPSPPS=1**.

5 RF Specifications

5.1. Cellular Network

5.1.1. Antenna Interface & Frequency Bands

The pin definition is shown below:

Table 32: Pin Definition of Cellular Network Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_MAIN	60	AIO	Main antenna interface	50 Ω impedance

Table 33: Operating Frequency

Operating Frequency	Transmit (MHz)	Receive (MHz)	Unit
LTE HD-FDD B1	1920–1980	2110–2170	MHz
LTE HD-FDD B2	1850–1910	1930–1990	MHz
LTE HD-FDD B3	1710–1785	1805–1880	MHz
LTE HD-FDD B4	1710–1755	2110–2155	MHz
LTE HD-FDD B5	824–849	869–894	MHz
LTE HD-FDD B8	880–915	925–960	MHz
LTE HD-FDD B12	699–716	729–746	MHz
LTE HD-FDD B13	777–787	746–756	MHz
LTE HD-FDD B17 [9]	704–716	734–746	MHz

[9] LTE HD-FDD B17 is supported by Cat NB2* only.

LTE HD-FDD B18	815–830	860–875	MHz
LTE HD-FDD B19	830–845	875–890	MHz
LTE HD-FDD B20	832–862	791–821	MHz
LTE HD-FDD B25	1850–1915	1930–1995	MHz
LTE HD-FDD B26 [10]	814–849	859–894	MHz
LTE HD-FDD B27 [10]	807–824	852–869	MHz
LTE HD-FDD B28	703–748	758–803	MHz
LTE HD-FDD B66	1710–1780	2110–2180	MHz

5.1.2. Tx Power

The Tx power of the module is presented in the following table.

Table 34: RF Output Power

Frequency Bands	Max. Tx Power	Min. Tx Power
LTE HD-FDD: B1/B2/B3/B4/B5/B8/B12/B13/B17 [9]/B18/B19/ B20/B25/B26 [10]/B27 [10]/B28/B66	23 dBm ±2.7 dB	< -39 dBm

5.1.3. Rx Sensitivity

The conducted Rx sensitivity of the module is presented in the following table.

Table 35: Conducted RF Receiving Sensitivity

Frequency Band	Primary	Diversity	Sensitivity (dBm)	
			Cat M1/3GPP	Cat NB1 [11]/3GPP
LTE HD-FDD B1	Supported	-	-105.3/-102.3	-114/-107.5
LTE HD-FDD B2			-105.3/-100.3	-114/-107.5

[10] LTE HD-FDD B26 and B27 are supported by Cat M1 only.
[11] LTE Cat NB1 receiving sensitivity without repetitions.

LTE HD-FDD B3	-104.3/-99.3	-113/-107.5
LTE HD-FDD B4	-105.3/-102.3	-114/-107.5
LTE HD-FDD B5	-105.8/-100.8	-115/-107.5
LTE HD-FDD B8	-105.8/-99.8	-115/-107.5
LTE HD-FDD B12	-105.3/-99.3	-114/-107.5
LTE HD-FDD B13	-105.3/-99.3	-114/-107.5
LTE HD-FDD B17 [12]	-	-114/-107.5
LTE HD-FDD B18	-106.3/-102.3	-115/-107.5
LTE HD-FDD B19	-106.3/-102.3	-115/-107.5
LTE HD-FDD B20	-105.8/-99.8	-114/-107.5
LTE HD-FDD B25	-104.8/-100.3	-114/-107.5
LTE HD-FDD B26 [13]	-106.3/-100.3	-
LTE HD-FDD B27 [13]	-106.3/-100.8	-
LTE HD-FDD B28	-105.8/-100.8	-114/-107.5
LTE HD-FDD B66	-104.8/-101.8	-114/-107.5

5.1.4. Reference Design

It is recommended to reserve a π-type matching circuit for better RF performance, and the π-type matching components (R1, C1 and C2) should be placed as close to the antenna as possible. The capacitors are not mounted by default.

[12] LTE HD-FDD B17 is supported by Cat NB2* only.
[13] LTE HD-FDD B26 and B27 are supported by Cat M1 only.

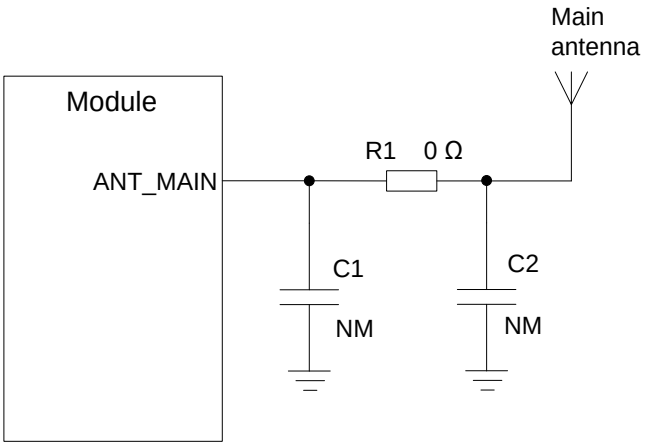


Figure 28: Reference Circuit of Main Antenna Interface

5.2. GNSS

BG950A-GL module features a fully integrated GNSS solution that supports GPS and GLONASS. BG951A-GL module has an independent GNSS solution that supports GPS, GLONASS, BDS, Galileo and QZSS.

The modules support standard *NMEA-0183* protocol. BG950A-GL outputs GNSS NMEA sentences via the CLI UART interfaces. BG951A-GL outputs NMEA sentences via the GNSS UART interface. Data update rate for both modules: 1–10 Hz; 1 Hz by default.

GNSS engine is switched off by default. It must be switched on via AT command. BG950A-GL does not support concurrent operation of LTE and GNSS, while BG951A-GL does. For more details about GNSS engine technology and configurations, see ***document [4]***.

5.2.1. Antenna Interface & Frequency Bands

The pin definition, frequency bands, and performance of GNSS antenna interface are presented in the following table shows.

Table 36: Pin Definition of GNSS Antenna Interface

Pin Name	Pin No.	I/O	Description	Comment
ANT_GNSS	49	AI	GNSS antenna interface	50 Ω impedance

Table 37: BG950A-GL GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz

Table 38: BG951A-GL GNSS Frequency

Type	Frequency	Unit
GPS	1575.42 ±1.023	MHz
GLONASS	1597.5–1605.8	MHz
BDS	1561.098 ±2.046	MHz
Galileo	1575.42 ±2.046	MHz
QZSS	1575.42 ±1.023	MHz

5.2.2. GNSS Performance

Table 39: BG950A-GL GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Cold start	Autonomous	-145	dBm
	Reacquisition	Autonomous	-154	
	Tracking	Autonomous	-159	
TTFF (GNSS)	Cold start @ open sky	Autonomous	29.42	s
		XTRA enabled	TBD	
	Warm start @ open sky	Autonomous	28.38	
		XTRA enabled	TBD	
	Hot start @ open sky	Autonomous	1.07	
		XTRA enabled	TBD	

Accuracy (GNSS)	CEP-50	Autonomous @ open sky	2.0	m

Table 40: BG951A-GL GNSS Performance

Parameter	Description	Conditions	Typ.	Unit
Sensitivity (GNSS)	Acquisition	Autonomous	-145	dBm
	Reacquisition	Autonomous	-145	
	Tracking	Autonomous	-160	
TTFF (GNSS)	Cold start @ open sky	Autonomous	34	s
		XTRA enabled	TBD	
	Warm start @ open sky	Autonomous	36	
		XTRA enabled	TBD	
	Hot start @ open sky	Autonomous	1	
		XTRA enabled	TBD	
Accuracy (GNSS)	CEP-50	Autonomous @ open sky	0.76	m

NOTE

1. Tracking sensitivity: the minimum GNSS signal power at which the module can maintain a lock (keep positioning for at least 3 minutes continuously).
2. Reacquisition sensitivity: the minimum GNSS signal power required for the module to maintain a lock within 3 minutes after loss of lock.
3. Acquisition sensitivity: the minimum GNSS signal power at which the module can fix a position successfully within 3 minutes after executing cold start command.

5.2.3. Reference Design

The following is the reference design of GNSS antenna.

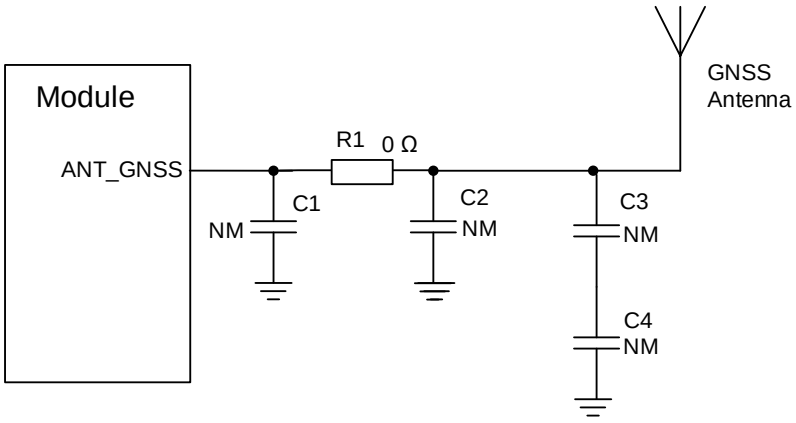


Figure 29: Reference Design of GNSS Antenna Interface

NOTE

The module is designed with a built-in LNA, and supports passive GNSS antennas only. Active antennas and external LNAs are not supported.

5.3. Layout Guidelines

The following layout guidelines should be taken into account in application designs.

- Maximize the distance between the GNSS antenna and the main antenna.
- Digital circuits such as (U)SIM card, USB interface, camera module, display connector, and SD card should be kept away from antennas.
- Use ground vias around the GNSS trace and sensitive analog signal traces to provide coplanar isolation and protection.
- Keep 50 Ω characteristic impedance for the ANT_GNSS trace.

Refer to ***Chapter 5.2*** for GNSS antenna reference design and antenna installation information.

5.4. RF Routing Guidelines

For user's PCB, the characteristic impedance of all RF traces should be 50 Ω. The impedance of the RF traces is usually determined by trace width (W), the materials' dielectric constant, the height from the reference ground to the signal layer (H), and the space between RF traces and grounds (S). Microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs of microstrip or coplanar waveguides with different PCB structures.

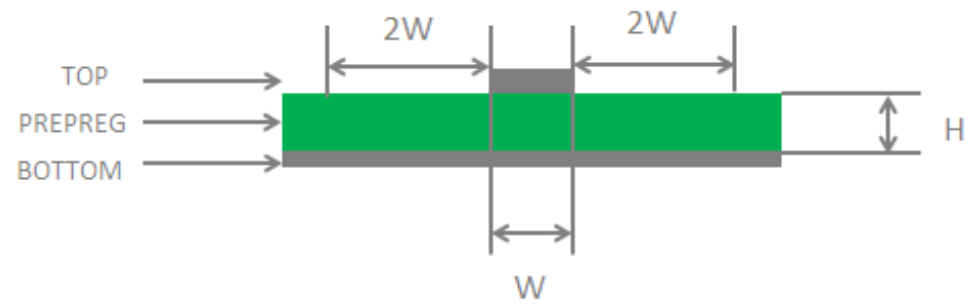


Figure 30: Microstrip Design on a 2-Layer PCB

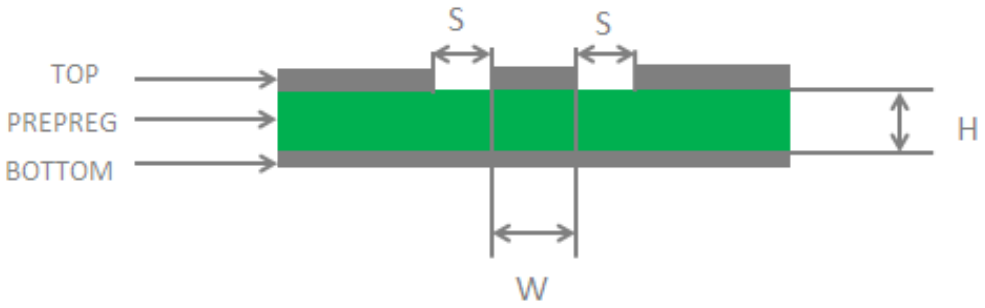


Figure 31: Coplanar Waveguide Design on a 2-Layer PCB

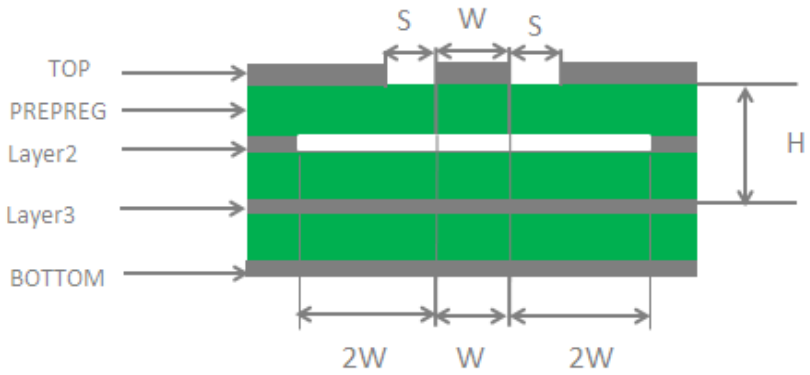


Figure 32: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

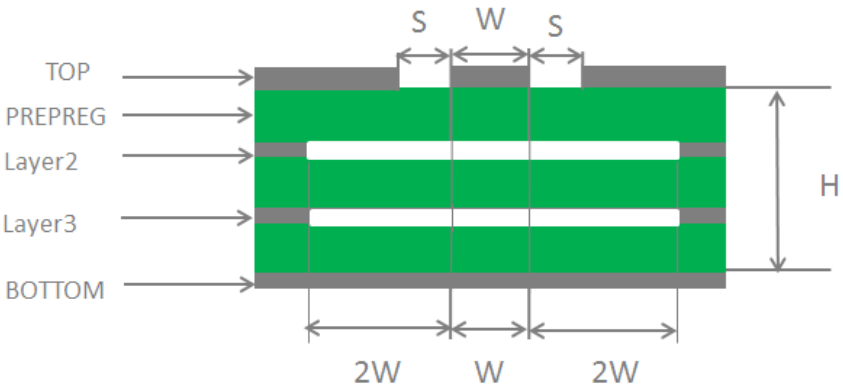


Figure 33: Coplanar Waveguide Design on a 4-Layer PCB (Layer 4 as Reference Ground)

To ensure RF performance and reliability, follow the principles below in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces to 50 Ω.
- The GND pins adjacent to RF pins should not be designed as thermal relief pads, and should be fully connected to ground.
- The distance between the RF pins and the RF connector should be as short as possible and all the right-angle traces should be changed to curved ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground could help to improve RF performance. The distance between the ground vias and RF traces should be at least two times the width of RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details about RF layout, see ***document [5]***.

5.5. Antenna Design Requirements

Table 41: Antenna Design Requirements

Antenna Type	Requirements
GNSS	Must be a passive antenna Frequency range: 1559–1609 MHz Polarization: RHCP or linear VSWR: < 2 (Typ.) Passive antenna gain: > 0 dBi
LTE	VSWR: ≤ 2

	Efficiency: > 30 % Gain: 1 dBi Max input power: 50 W Input impedance: 50 Ω Polarization: vertical Cable insertion loss: − **< 1 dB:** LB (< 1 GHz) − **< 1.5 dB**: MB (1–2.3 GHz)

5.6. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

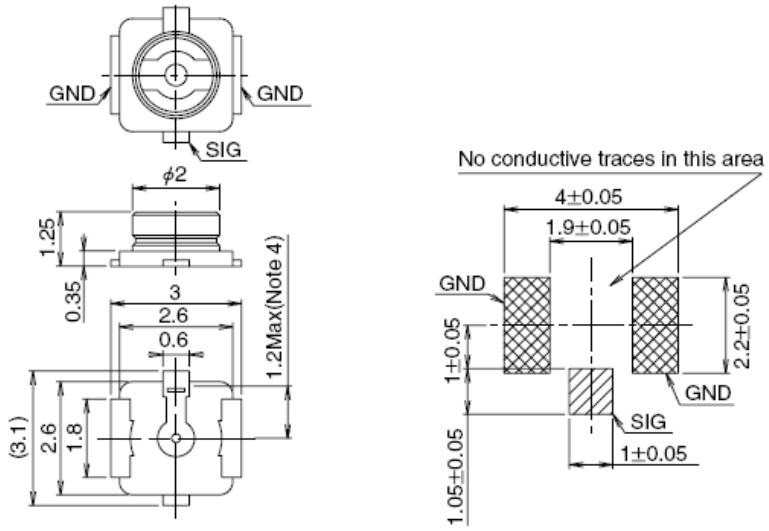


Figure 34: Dimensions of the Receptacle (Unit: mm)

The mated plugs listed in the following figure can be used to match the U.FL-R-SMT connector.

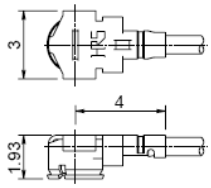
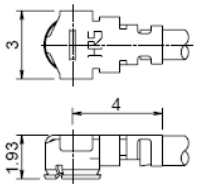
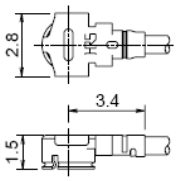
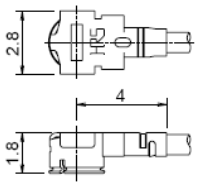
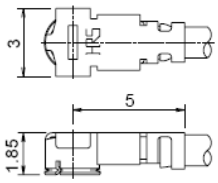
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 35: Specifications of Mated Plugs

The following figure describes the space factor of the mated connector.

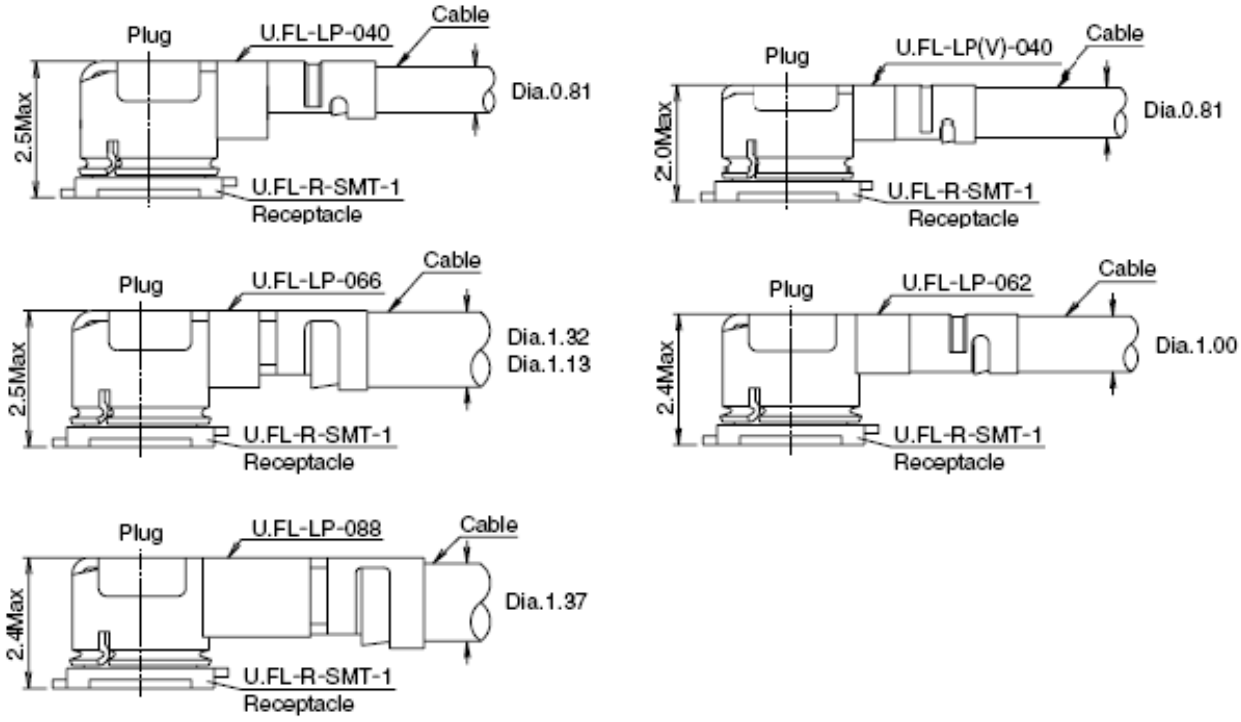


Figure 36: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

6 Reliability and Electrical Characteristics

6.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 42: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT_RF/VBAT_BB	-0.2	4.5	V
USB_VBUS	-0.3	5.5	V
Voltage at Digital Pins	-0.3	2.0	V

6.2. Power Supply Ratings

Table 43: Power Supply Ratings

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
VBAT_BB/ VBAT_RF	Power supply for the module's baseband part/RF part	The actual input voltages must stay between the minimum and maximum values.	2.2	3.3	4.35	V
USB_VBUS	USB connection detect	-	-	5.0	-	V

6.3. Power Consumption

6.3.1. BG950A-GL Power Consumption

Table 44: BG950A-GL Power Consumption (Power Supply: 3.3 V, Room Temperature)

Description	Conditions	Avg.	Max.	Unit
Leakage	Power-off @ USB/UART disconnected	1.5	-	μA
PSM	PSM @ USB/UART disconnected	1.5	-	μA
Rock bottom	**AT+CFUN=0** @ Sleep mode	39	-	μA
Sleep mode (USB disconnected)	LTE Cat M1 DRX = 1.28 s	1.1	-	mA
	LTE Cat NB1 DRX = 1.28 s	2.2	-	mA
	LTE Cat M1 e-I-DRX = 40.96 s @ PTW = 1.28 s, DRX = 1.28 s	0.09	-	mA
	LTE Cat M1 e-I-DRX = 40.96 s @ PTW = 2.56 s, DRX = 1.28 s	0.12	-	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 1.28 s, DRX = 1.28 s	0.07	-	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	0.09	-	mA
	LTE Cat NB1 e-I-DRX = 40.96 s @ PTW = 2.56 s, DRX = 1.28 s	0.19	-	mA
	LTE Cat NB1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	0.15	-	mA
Idle state	LTE Cat M1 DRX = 1.28 s	15.0	-	mA
	LTE Cat NB1 DRX = 1.28 s	16.0	-	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	15.0	-	mA
	LTE Cat NB1 e-I-DRX = 81.92 s	15.0	-	mA

	@ PTW = 2.56 s, DRX = 1.28 s			
LTE Cat M1 data transfer (GNSS OFF)	LTE HD-FDD B1 @ 23.01 dBm	242	657	mA
	LTE HD-FDD B2 @ 23.04 dBm	224	596	mA
	LTE HD-FDD B3 @ 23.03 dBm	207	535	mA
	LTE HD-FDD B4 @ 23.03 dBm	208	533	mA
	LTE HD-FDD B5 @ 23.08 dBm	208	544	mA
	LTE HD-FDD B8 @ 23.02 dBm	220	607	mA
	LTE HD-FDD B12 @ 23.01 dBm	204	521	mA
	LTE HD-FDD B13 @ 23.03 dBm	199	514	mA
	LTE HD-FDD B18 @ 23.04 dBm	201	528	mA
	LTE HD-FDD B19 @ 23.16 dBm	209	548	mA
	LTE HD-FDD B20 @ 23.02 dBm	211	555	mA
	LTE HD-FDD B25 @ 23.06 dBm	236	628	mA
	LTE HD-FDD B26 @ 23.07 dBm	209	544	mA
	LTE HD-FDD B27 @ 23.09 dBm	201	519	mA
	LTE HD-FDD B28 @ 22.99 dBm	200	504	mA
	LTE HD-FDD B66 @ 22.78 dBm	209	536	mA
LTE Cat NB1 data transfer (GNSS OFF)	LTE HD-FDD B1 @ 23.19 dBm	247	700	mA
	LTE HD-FDD B2 @ 23.01 dBm	222	588	mA
	LTE HD-FDD B3 @ 23.10 dBm	208	548	mA
	LTE HD-FDD B4 @ 23.09 dBm	203	541	mA
	LTE HD-FDD B5 @ 23.03 dBm	204	532	mA
	LTE HD-FDD B8 @ 23.10 dBm	223	608	mA
	LTE HD-FDD B12 @ 23.09 dBm	194	529	mA
	LTE HD-FDD B13 @ 23.20 dBm	185	499	mA
	LTE HD-FDD B17 @ 23.06 dBm	191	515	mA

	LTE HD-FDD B18 @ 23.19 dBm	197	530	mA
	LTE HD-FDD B19 @ 23.20 dBm	200	541	mA
	LTE HD-FDD B20 @ 23.15 dBm	209	570	mA
	LTE HD-FDD B25 @ 23.17 dBm	220	585	mA
	LTE HD-FDD B28 @ 23.12 dBm	187	506	mA
	LTE HD-FDD B66 @ 22.82 dBm	205	554	mA

6.3.2. BG951A-GL Power Consumption

Table 45: BG951A-GL Power Consumption (Power Supply: 3.3 V, Room Temperature)

Description	Conditions	Avg.	Max.	Unit
Leakage	Power-off @ USB/UART disconnected	1.5	-	μA
PSM	PSM @ USB/UART disconnected	1.5	-	μA
Rock bottom	**AT+CFUN=0** @ Sleep mode	42	-	μA
Sleep mode (USB disconnected)	LTE Cat M1 DRX = 1.28 s	1.1	-	mA
	LTE Cat NB1 DRX = 1.28 s	2.2	-	mA
	LTE Cat M1 e-I-DRX = 40.96 s @ PTW = 1.28 s, DRX = 1.28 s	0.09	-	mA
	LTE Cat M1 e-I-DRX = 40.96 s @ PTW = 2.56 s, DRX = 1.28 s	0.12	-	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 1.28 s, DRX = 1.28 s	0.08	-	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	0.10		mA
	LTE Cat NB1 e-I-DRX = 40.96 s @ PTW = 2.56 s, DRX = 1.28 s	0.18	-	mA
	LTE Cat NB1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	0.14	-	mA

Idle state	LTE Cat M1 DRX = 1.28 s	17.0	-	mA
	LTE Cat NB1 DRX = 1.28 s	17.0	-	mA
	LTE Cat M1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	16.0	-	mA
	LTE Cat NB1 e-I-DRX = 81.92 s @ PTW = 2.56 s, DRX = 1.28 s	16.0	-	mA
LTE Cat M1 data transfer (GNSS OFF)	LTE HD-FDD B1 @ 23.01 dBm	242	657	mA
	LTE HD-FDD B2 @ 23.04 dBm	224	596	mA
	LTE HD-FDD B3 @ 23.03 dBm	207	535	mA
	LTE HD-FDD B4 @ 23.03 dBm	208	533	mA
	LTE HD-FDD B5 @ 23.08 dBm	208	544	mA
	LTE HD-FDD B8 @ 23.02 dBm	220	607	mA
	LTE HD-FDD B12 @ 23.01 dBm	204	521	mA
	LTE HD-FDD B13 @ 23.03 dBm	199	514	mA
	LTE HD-FDD B18 @ 23.04 dBm	201	528	mA
	LTE HD-FDD B19 @ 23.16 dBm	209	548	mA
	LTE HD-FDD B20 @ 23.02dBm	211	555	mA
	LTE HD-FDD B25 @ 23.06 dBm	236	628	mA
	LTE HD-FDD B26 @ 23.07 dBm	209	544	mA
	LTE HD-FDD B27 @ 23.09 dBm	201	519	mA
	LTE HD-FDD B28 @ 22.99 dBm	200	504	mA
	LTE HD-FDD B66 @ 22.78 dBm	209	536	mA
LTE Cat NB1 data transfer (GNSS OFF)	LTE HD-FDD B1 @ 23.19 dBm	247	700	mA
	LTE HD-FDD B2 @ 23.01 dBm	222	588	mA
	LTE HD-FDD B3 @ 23.10 dBm	208	548	mA
	LTE HD-FDD B4 @ 23.09 dBm	203	541	mA
	LTE HD-FDD B5 @ 23.03 dBm	204	532	mA

	LTE HD-FDD B8 @ 23.10 dBm	223	608	mA
	LTE HD-FDD B12 @ 23.09 dBm	194	529	mA
	LTE HD-FDD B13 @ 23.20 dBm	185	499	mA
	LTE HD-FDD B17 @ 23.06 dBm	191	515	mA
	LTE HD-FDD B18 @ 23.19 dBm	197	530	mA
	LTE HD-FDD B19 @ 23.20 dBm	200	541	mA
	LTE HD-FDD B20 @ 23.15 dBm	209	570	mA
	LTE HD-FDD B25 @ 23.17 dBm	220	585	mA
	LTE HD-FDD B28 @ 23.12 dBm	187	506	mA
	LTE HD-FDD B66 @ 22.82 dBm	205	554	mA

6.3.3. GNSS Power Consumption

Table 46: BG950A-GL GNSS Power Consumption

Description	Conditions	Typ.	Unit
Searching **(AT+CFUN=0)**	Cold start @ Passive antenna	48.19	mA
	Hot start @ Passive antenna	48.63	mA
	Lost state @ Passive antenna	47.97	mA
Tracking **(AT+CFUN=0)**	Instrument environment @ Passive antenna	48.44	mA
	Open sky @ Real network, Passive antenna	TBD	mA

Table 47: BG951A-GL GNSS Power Consumption

Description	Conditions	Typ.	Unit
GNSS startup non-positioning **(AT+CFUN=0** & **AT+QSCLK=2)**	Instrument environment @ Passive antenna	3.62	mA
Searching **(AT+CFUN=0)**	Cold start @ Passive antenna	21.51	mA
	Hot start @ Passive antenna	20.07	mA

	Lost state @ Passive antenna	20.99	mA
Tracking **(AT+CFUN=0)**	Instrument environment @ Passive antenna	15.51	mA
	Open sky @ Real network, Passive antenna	16.50	mA

6.4. Digital I/O Characteristic

Table 48: 1.8 V Digital I/O Requirements – (U)SIM

Parameter	Description	Min.	Max.	Unit
USIM_VDD	Power supply	1.7	1.9	V
V_{IH}	Input high voltage	1.26	2.0	V
V_{IL}	Input low voltage	-0.2	0.54	V
V_{OH}	Output high voltage	1.44	2.0	V
V_{OL}	Output low voltage	-0.2	0.36	V

Table 49: 1.8 V Digital I/O Requirements – Others

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	1.26	2.0	V
V_{IL}	Input low voltage	-0.2	0.54	V
V_{OH}	Output high voltage	1.44	2.0	V
V_{OL}	Output low voltage	-0.2	0.36	V

6.5. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly, and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 50: Electrostatics Discharge Characteristics (Temperature: 25 °C, Humidity: 45 %)

Tested Interfaces	Contact Discharge	Air Discharge	Unit
VBAT, GND	±8	±12	kV
Main Antenna Interfaces	±5	±10	kV
GNSS Antenna Interfaces	±5	±8	kV

6.6. Operating and Storage Temperatures

Table 51: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [14]	-35	+25	+75	°C
Extended Temperature Range [15]	-40	-	+85	°C
Storage Temperature Range	-40	-	+90	°C

[14] Within the operating temperature range, the module meets 3GPP specifications.
[15] Within the extended temperature range, the module retains the ability to establish and maintain functions such as SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified 3GPP tolerances. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

7 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeters (mm). The dimensional tolerances are ±0.2 mm, unless otherwise specified.

7.1. Top and Side View Dimensions

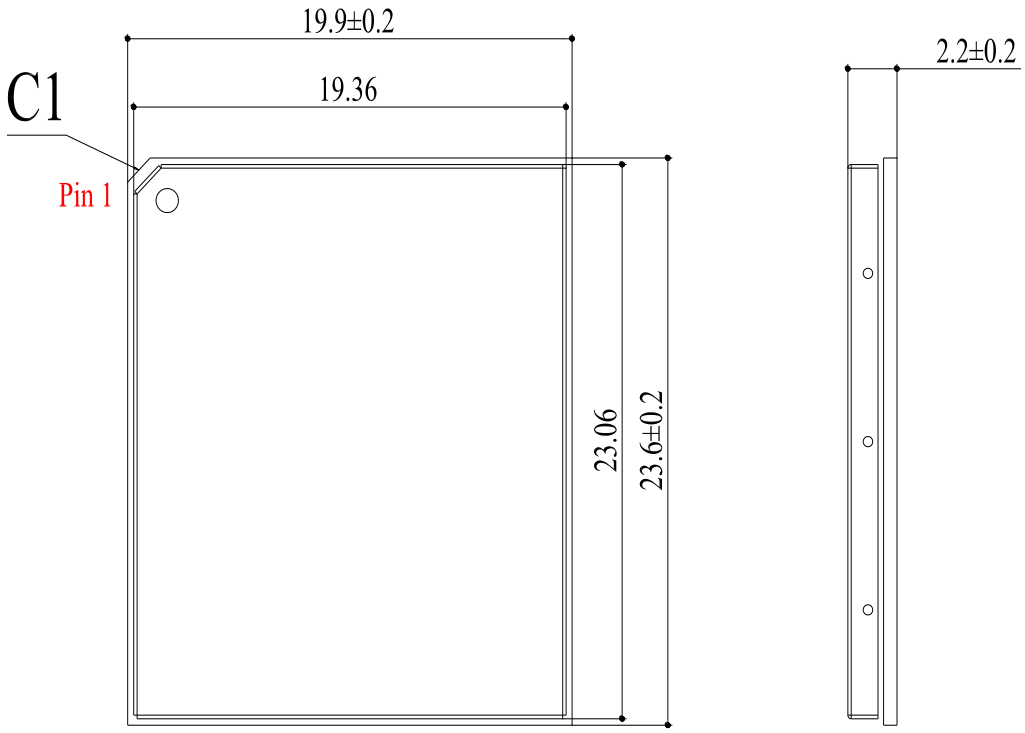


Figure 37: Module Top and Side Dimensions (Unit: mm)

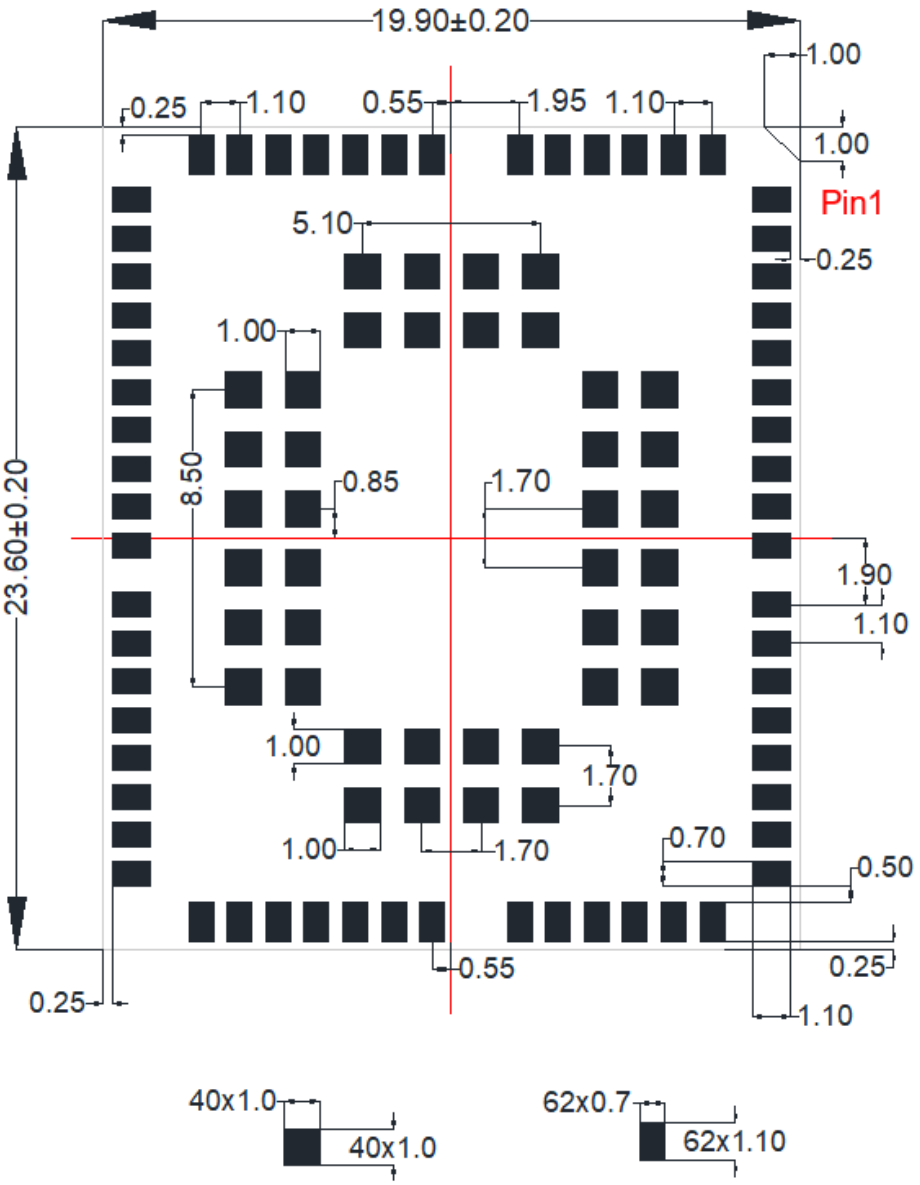


Figure 38: Module Bottom Dimensions (Bottom View, Unit: mm)

NOTE

The package warpage level of the module conforms to the *JEITA ED-7306* standard.

7.2. Recommended Footprint

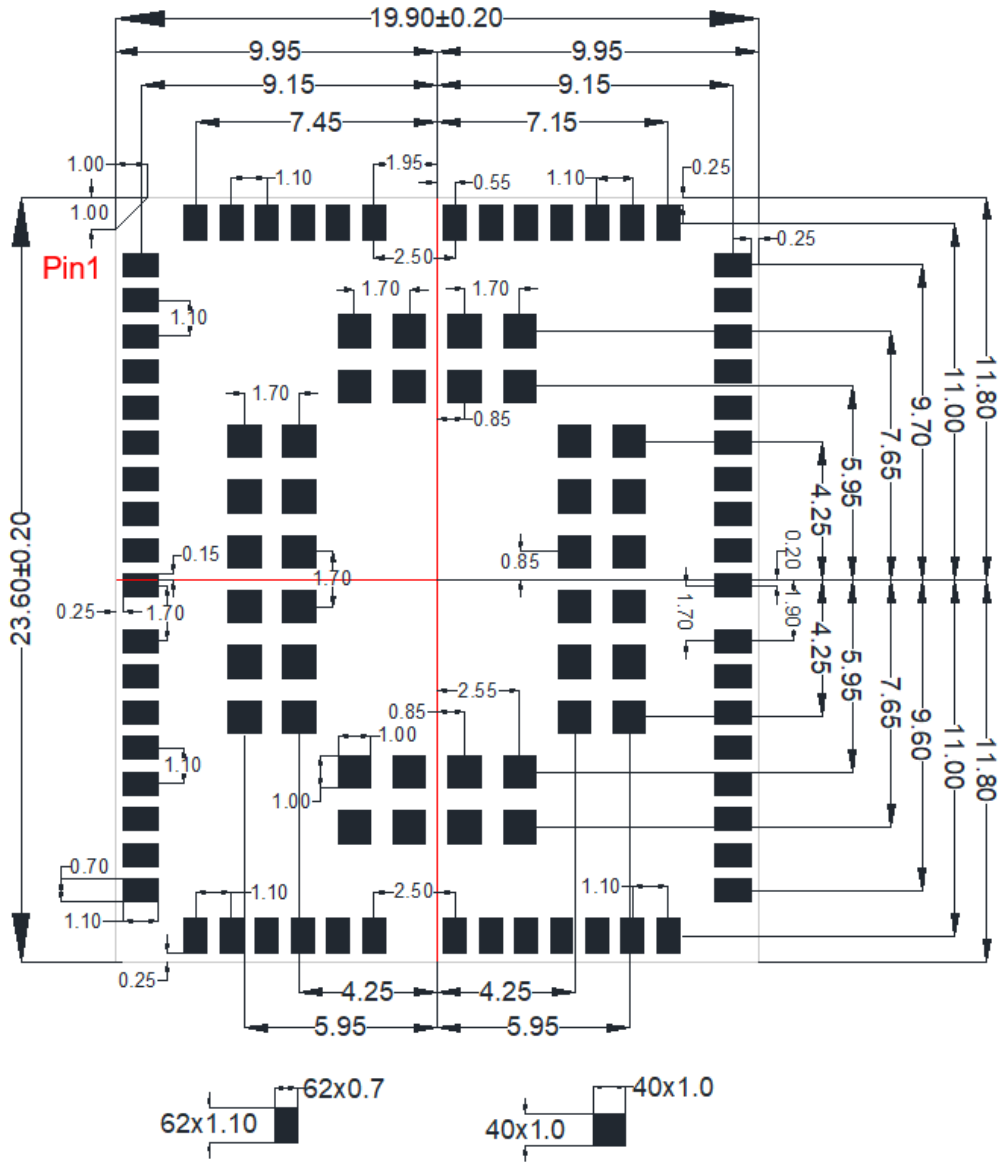


Figure 39: Recommended Footprint (Top View, Unit: mm)

NOTE

1. Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.
2. All reserved pins must be kept open.
3. For stencil design requirements of the module, see ***document [6].***

7.3. Top and Bottom Views

Figure 40: Top & Bottom Views of BG950A-GL & BG951A-GL

NOTE

Images above are for illustrative purposes only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

8 Storage, Manufacturing & Packaging

8.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [16] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[16] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. And do not remove the packages of tremendous modules if they are not ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. All modules must be soldered to PCB within 24 hours of the baking, otherwise put them in the drying oven. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

8.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the stencil surface, thus making the paste fill the stencil openings and then penetrate the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, 0.13–0.15 mm stencil thickness for the module is recommended. For more details, see ***document [6].***

The peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid module damage caused by repeated heating, it is strongly recommended that the module should be mounted only after reflow soldering of the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

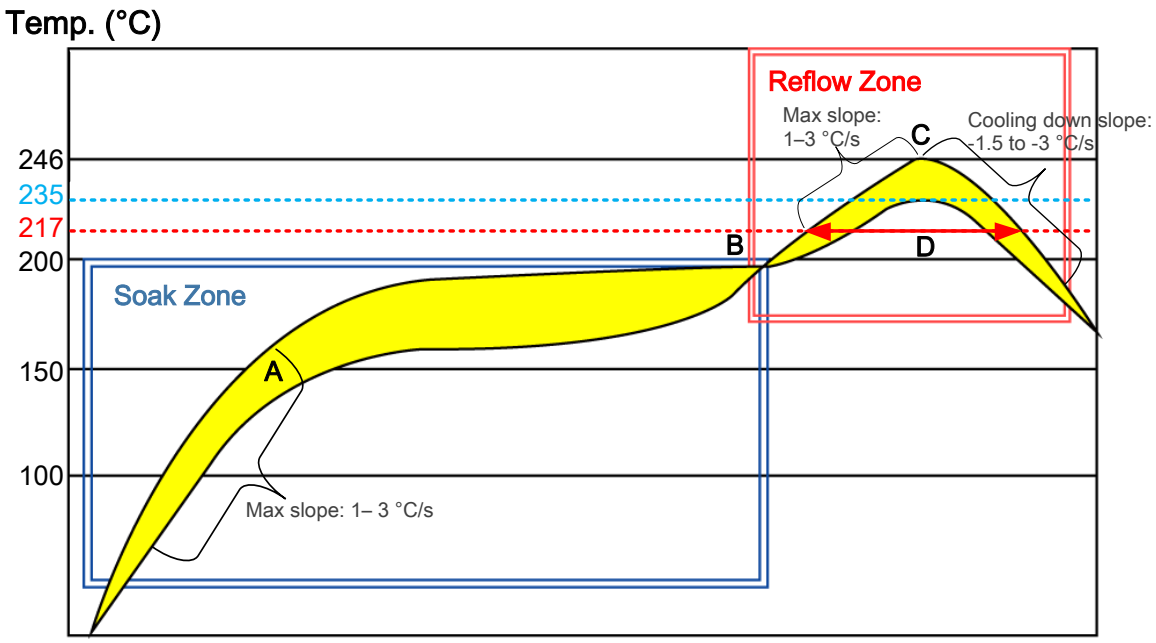


Figure 41: Recommended Reflow Soldering Thermal Profile

Table 52: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Max slope	1–3 °C/s
Reflow time (D: over 217 °C)	40–70 s
Max temperature	235–246 °C
Cooling down slope	-1.5 to 3 °C/s
Reflow Cycle	
Max reflow cycle	1

NOTE

1. If the module requires conformal coating, DO NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
2. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
3. Due to the SMT process complexity, please contact Quectel Technical Support in advance regarding any situation that you are not sure about, or any process (e.g., selective soldering, ultrasonic soldering) that is not mentioned in ***document [6].***

8.3. Packaging Specifications

The module is delivered in a tape carrier packaging and details are as follows:

8.3.1. Carrier Tape

Dimension details:

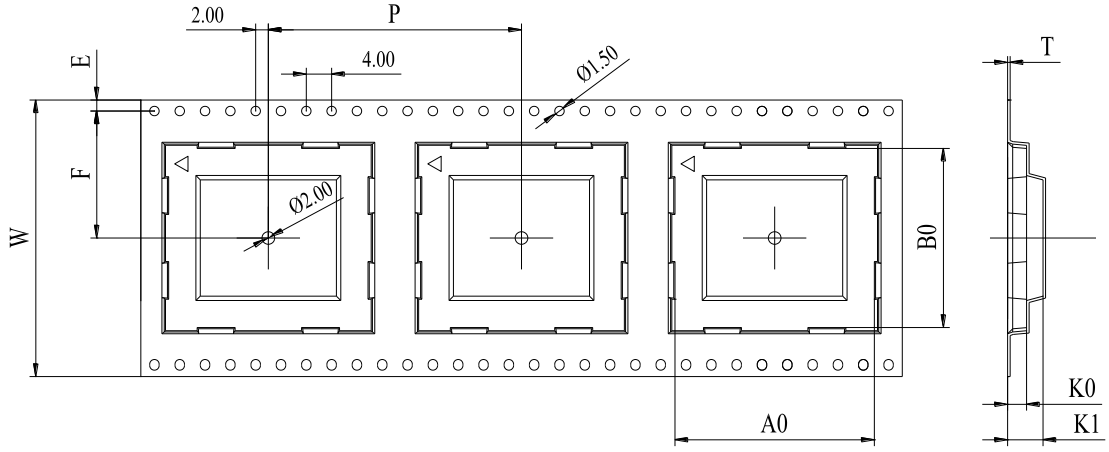


Figure 42: Carrier Tape Dimension Drawing

Table 53: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
44	32	0.35	20.2	24	3.15	6.65	20.2	1.75

8.3.2. Plastic Reel

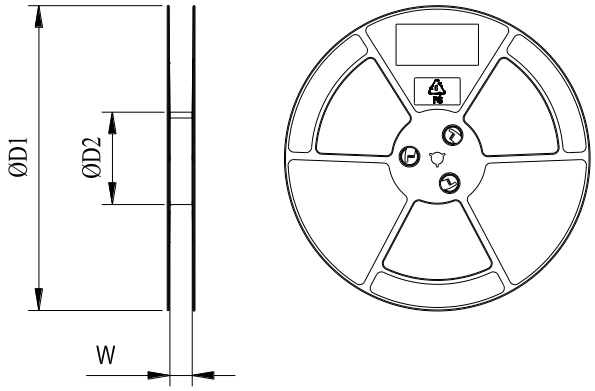
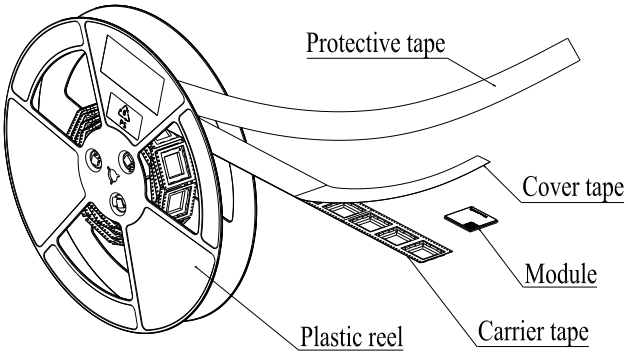


Figure 43: Plastic Reel Dimension Drawing

Table 54: Plastic Reel Dimension Table (Unit: mm)

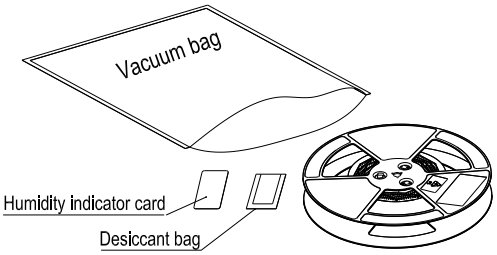
øD1	øD2	W
330	100	44.5

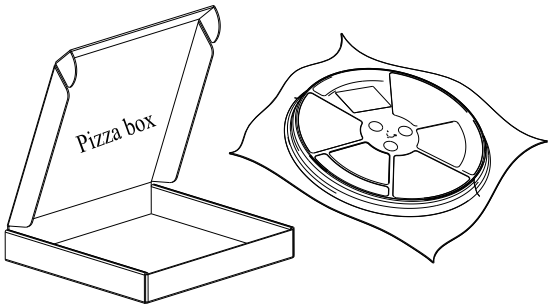
8.3.3. Packing Process



Place the module onto the carrier tape and use the cover tape to cover them; then wind the heat-sealed carrier tape on the plastic reel and use the protective tape for protection. One plastic reel can load 250 modules.

Place the packaged plastic reel, humidity indicator card and desiccant bag inside a vacuum bag, then vacuumize it.





Place the vacuum-packed plastic reel inside a pizza box.

Place 4 pizza boxes inside 1 carton and seal it. One carton can pack 1000 modules.

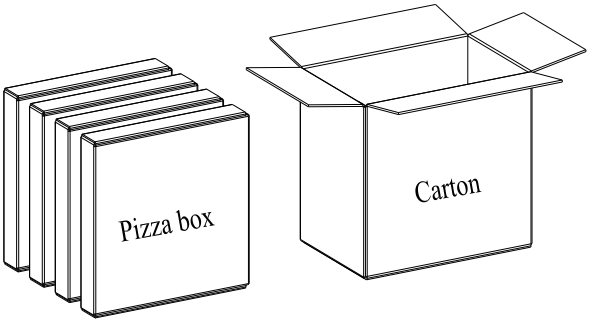


Figure 44: Packaging Process

9 Appendix References

Table 55: Related Documents

Document Name
[1] Quectel_UMTS&LTE_EVB_User_Guide
[2] Quectel_BG77xA-GL&BG95xA-GL_QCFG_AT_Commands_Manual
[3] Quectel_BG77xA-GL&BG95xA-GL_AT_Commands_Manual
[4] Quectel_BG770A-GL&BG95xA-GL_GNSS_Application_Note
[5] Quectel_RF_Layout_Application_Note
[6] Quectel_Module_Secondary_SMT_Application_Note
[7] Quectel_BG950A-GL&BG951A-GL_TE-A_User_Guide

Table 56: Terms and Abbreviations

Abbreviation	Description
ADC	Analog to Digital Converter
BDS	BeiDou Navigation Satellite System
Balun	Balanced to Unbalanced
bps	bit(s) per second
CHAP	Challenge Handshake Authentication Protocol
CoAP	Constrained Application Protocol
CTS	Clear to Send
DFOTA	Delta Firmware Upgrade Over-the-Air
DL	Downlink

DRX	Discontinuous Reception
EGSM	Extended GSM (Global System for Mobile Communications)
e-I-DRX	Extended Idle Mode Discontinuous Reception
EPC	Evolved Packet Core
ESD	Electrostatic Discharge
EVB	Evaluation Board
FDD	Frequency Division Duplex
FTP(S)	FTP over SSL
GNSS	Global Navigation Satellite System
GLONASS	Global Navigation Satellite System (Russia)
GPIO	General-Purpose Input/Output
GPS	Global Positioning System
GRFC	Generic RF Controller
HD	Half Duplex
HSS	Home Subscriber Server
I/O	Input/Output
I2C	Inter-Integrated Circuit
Inom	Nominal Current
LDO	Low-Dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
LPF	Low Pass Filter
LPWA	Low-Power Wide-Area (Network)
LTE	Long Term Evolution

LwM2M	Lightweight M2M
ME	Mobile Equipment
MO	Mobile Originated
MQTT	Message Queuing Telemetry Transport
MSL	Moisture Sensitivity Levels
MT	Mobile Terminated
NITZ	Network Identity and Time Zone
NMEA	NMEA (National Marine Electronics Association) 0183 Interface Standard
PA	Power Amplifier
PAP	Password Authentication Protocol
PCB	Printed Circuit Board
PDU	Protocol Data Unit
PING	Packet Internet Groper
PMU	Power Management Unit
POS	Point of Sale
PPP	Point-to-Point Protocol
PSM	Power Saving Mode
RAU	Routing Area Update
RF	Radio Frequency
RFIC	Radio Frequency Integrated Circuit
RHCP	Right Hand Circularly Polarized
RoHS	Restriction of Hazardous Substances
RTS	Request to Send
SAW	Surface Acoustic Wave
SMD	Surface Mount Device

SMS	Short Message Service
SSL	Secure Sockets Layer
TAU	Tracking Area Update
TCP	Transmission Control Protocol
TCXO	Temperature Complementary Crystal Oscillator
TLS	Transport Layer Security
TTFF	Time to First Fix
Tx	Transmit
UART	Universal Asynchronous Receiver/Transmitter
UDP	User Datagram Protocol
UL	Uplink
UE	User Equipment
URC	Unsolicited Result Code
(U)SIM	(Universal) Subscriber Identity Module
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
VSWR	Voltage Standing Wave Ratio