BC68 Hardware Design

LPWA Module Series

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About the Document

History

Revision	Date	Author	Description
1.0	2017-12-01	Brooke WANG/ Vick YANG	Initial
1.1	2018-09-21	Power JIN/ Glenn GE	1. Changed interface information and added OTDOA function (Table 2); 2. Updated the reference circuit of power supply with VBAT (Figure 4); 3. Updated level match design for 3.3V system (Figure 11); 4. Updated sketch map for RS-232 interface match (Figure 12); 5. Added content about manufacturing and soldering (Chapter 7.2); 6. Added the receiving sensitivity without retransmission (Table 17); 7. Updated the receiving sensitivity in retransmission (Table 18).
1.2	2019-01-10	Glenn GE	1. Updated the reference design of VCC level match for UART Application (Figure 11); 2. Updated the sketch map for RS-232 Interface Match (Figure 12); 3. Updated the description of NETLIGHT (Table 14); 4. Updated the value and description of current consumption of the module in PSM (Chapter 2.1, Chapter 2.2, Chapter 3.5 and Chapter 5.3); 5. Added Extended TBS/2 HARQ data transmission rate (Chapter 2.2).
1.3	2019-03-20	Glenn GE	1. Updated the following key features (Table 2): Deleted the “*” mark after ECID and OTDOA; Deleted Text* mode;

	2. Updated the module's current consumption in idle state (Table 24); 3. Updated the description of NETLIGHT working state (Table 14); 4. Updated top view figure of the module (Figure 27); 5. Updated the stencil thickness and peak reflow temperature (Chapter 7.2).

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1 Introduction

This document defines the BC68 module and describes its air interface and hardware interface which are connected to customers' applications.

This document can help customers to quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. Associated with application note and user guide, customers can use BC68 module to design and set up mobile applications easily.

1.1. Safety Information

The following safety precautions must be observed during all phases of the operation, such as usage, service or repair of any cellular terminal or mobile incorporating BC68 module. Manufacturers of the cellular terminal should send the following safety information to users and operating personnel, and incorporate these guidelines into all manuals offered with the product. Otherwise, Quectel assumes no liability for the customers' failure to comply with these precautions.

	Full attention must be always paid to driving in order to avoid distracted driving. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.
	Switch off the cellular terminals or mobiles before boarding an aircraft. Operating wireless devices in an aircraft is forbidden to prevent interference with aircraft systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the flight attendants for more restrictions on the use of wireless devices on boarding the aircraft.
	Wireless devices may cause interference with sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.
	Cellular terminals or mobiles operating over radio signals and cellular network cannot be guaranteed to connect to network in all possible conditions (for example, with unpaid bills or with an invalid (U)SIM card). When emergent help is needed in such conditions, please remember to use emergency call. In order to make or receive a call, the cellular terminal or mobile must be switched on within a service area with adequate cellular signal strength.

	The cellular terminal or mobile contains a transmitter and receiver. When it is on, it receives and delivers radio frequency signals. RF interference may occur if it is used close to TV set, radio, computer or other electric equipment.
	In locations with potentially explosive atmospheres, obey all posted signs turning off wireless devices such as your phone or other cellular terminals. Areas with potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, areas where the air contains chemicals or particles such as grain, dust or metal powders, etc.

2 Product Concept

2.1. General Description

BC68 is a high-performance NB-IoT module with low power consumption. It supports multiple frequency bands as illustrated in the table below. The module is designed to communicate with mobile network operators' infrastructures through the NB-IoT radio protocol (3GPP Rel.14).

Table 1: Frequency Bands of BC68

Band	Frequency
Band 1	@H-FDD 2100MHz
Band 3	@H-FDD 1800MHz
Band 8	@H-FDD 900MHz
Band 5	@H-FDD 850MHz
Band 20	@H-FDD 800MHz
Band 28	@H-FDD 700MHz

BC68 is an SMD type module with LCC package and comes with an ultra-compact profile of 17.7mm × 15.8mm × 2.0mm, making it able to be easily embedded. It satisfies nearly all the requirements for IoT applications, such as smart metering, bike sharing, smart parking, smart city, security and asset tracking, home appliances, agriculture and environment monitoring, etc.

Designed with power saving technique, BC68 consumes an ultra-low current of 3uA in PSM (Power Saving Mode).

The module fully complies with the RoHS directive of the European Union.

2.2. Key Features

The following table lists the detailed features of BC68.

Table 2: BC68 Key Features

Feature	Details
Power Supply	● Supply voltage: 3.1V~4.2V ● Typical supply voltage: 3.6V
Power Saving Mode	● Typical current consumption in PSM: 3uA
Transmitting Power	● 23dBm±2dB
Temperature Range	● Operation temperature range: -35°C ~ +75°C [1)] ● Extended temperature range: -40°C ~ +85°C [2)] ● Storage temperature range: -40°C ~ +90°C
USIM Interface	● Support 1.8V/3.0V USIM card
UART Interfaces	**Main port:** ● When used for AT command communication and data transmission, baud rates 4800bps, 9600bps (default), 57600bps, 115200bps, 230400bps and 460800bps are supported ● For firmware upgrading, baud rates 115200bps and 921600bps are supported **Debug port:** ● Used for firmware debugging ● Only supports 921600bps baud rate
Internet Protocol	● Supports IPv4/IPv6/UDP/CoAP/LWM2M/Non-IP/DTLS/TCP/MQTT
SMS	● PDU Mode ● Point-to-point MO and MT
Data Transmission	● Single-tone with a 15kHz/3.75kHz subcarrier spacing: 25.2kbps (DL)/15.625kbps (UL) ● Multi-tone with a 15kHz subcarrier spacing: 25.2kbps (DL)/54kbps (UL) ● Extended TBS/2 HARQ* with a 15kHz subcarrier spacing: 125kbps (DL)/150kbps (UL)
OTDOA	● Supports 3GPP R14
ECID	● Supports 3GPP R13

AT Commands	● 3GPP TS 27.007 V14.3.0 (2017-03) and Quectel enhanced AT commands
Physical Features	● Size: (17.7±0.15)mm × (15.8±0.15)mm × (2.0±0.20)mm ● Weight: 1.1g±0.2g
Firmware Upgrade	● Firmware upgrade via main port or DFOTA
Antenna Interface	● 50Ω impedance control
RoHS	● All hardware components are fully compliant with EU RoHS directive

NOTES

1. [1] Within the operation temperature range, the module meets 3GPP specifications.
2. [2] Within the extended temperature range, the module remains the ability to establish and maintain functions such as SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network will not be influenced. While there may be several parameters, such as P_{out}, reducing in value and exceeding the specified tolerances of 3GPP. When the temperature returns to the normal operating temperature levels, the module will meet 3GPP specifications again.
3. "*" means under development.

2.3. Functional Diagram

The following figure shows a block diagram of BC68 and illustrates the major functional parts.

- Radio frequency
- Baseband
- Power management
- Peripheral interfaces

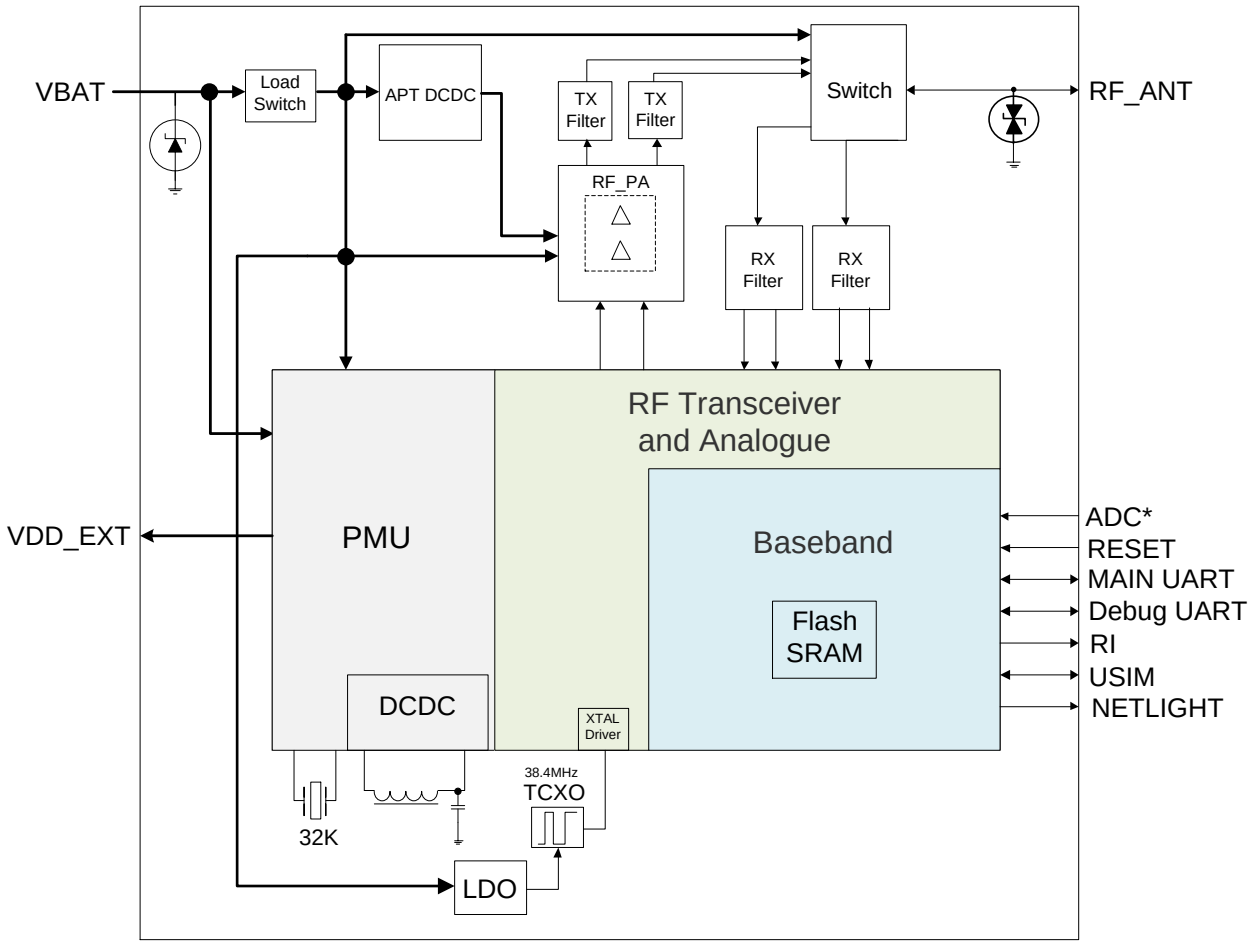


Figure 1: Functional Diagram

NOTE

"*" means under development.

2.4. Development Board

In order to help customers to develop applications with BC68 conveniently, Quectel supplies the development board (BC68-TE-B), Micro-USB cable, antenna and other peripherals to control or test the module. For more details, please refer to ***document [1]***.

3 Application Interfaces

3.1. General Description

BC68 is an SMD type module with 44 LCC pads and 14 LGA pads. The later chapters provide detailed descriptions of these pins:

- Power supply
- UART interfaces
- USIM interface
- ADC interface*
- RI behaviors
- Network status indication

NOTE

"*" means under development.

3.2. Pin Assignment

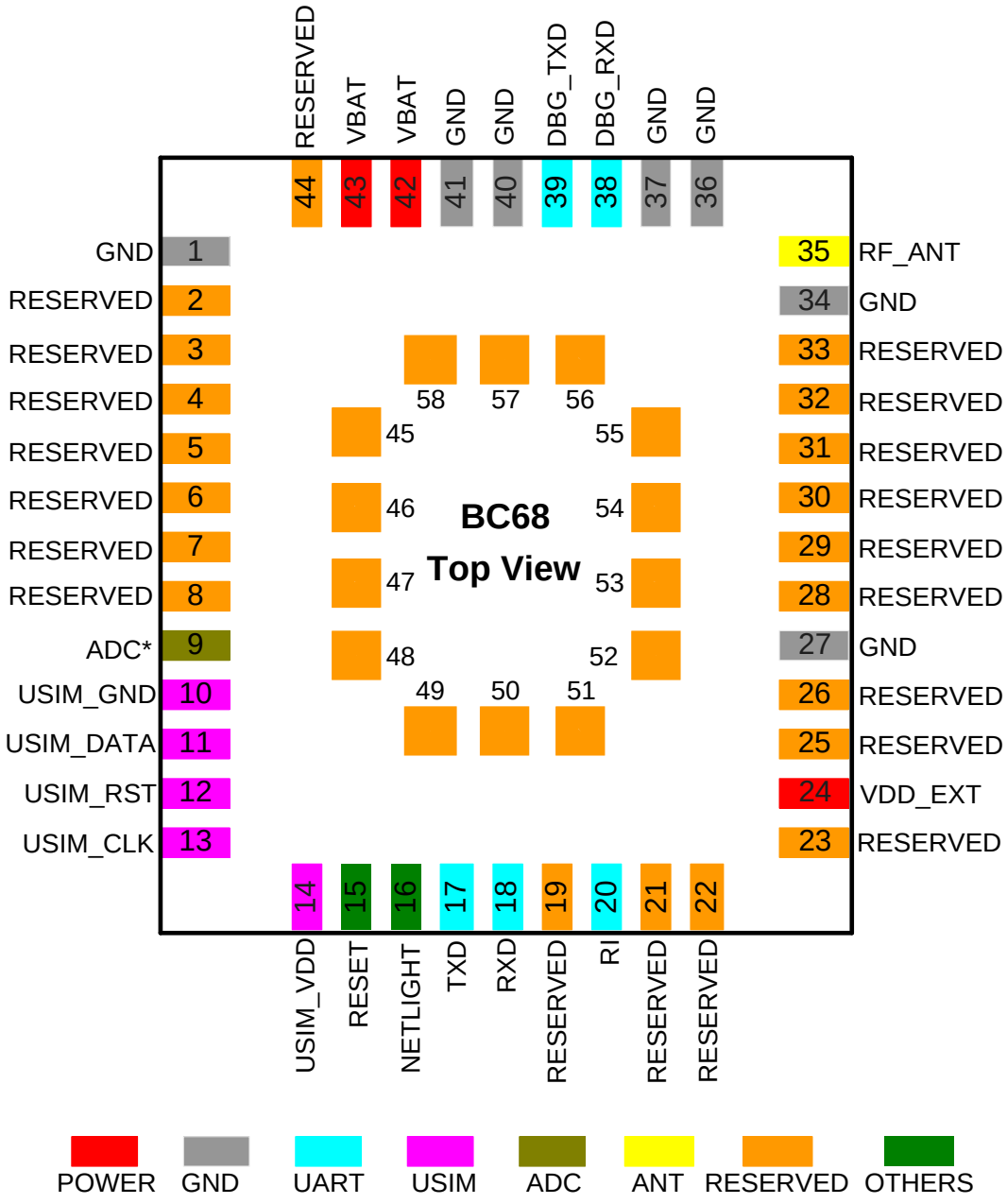


Figure 2: Pin Assignment

NOTES

1. All reserved pins should be kept unconnected.
2. "*" means under development.

3.3. Pin Description

The following tables show the pin definition and description of BC68.

Table 3: I/O Parameter Definition

Type	Description
IO	Bidirectional
DI	Digital input
DO	Digital output
PI	Power input
PO	Power output
AI	Analog input
AO	Analog output

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	42, 43	PI	Main power supply: VBAT=3.1V~4.2V	Vmax=4.2V Vmin=3.1V Vnorm=3.6V	The power supply must be able to provide sufficient current up to 0.5A.
VDD_EXT	24	PO	3.0V output power supply for external circuits	Vnorm=3.0V $I_O$max=20mA (1mA in PSM)	Used for external I/O ports with weak pull-ups and a 2.2uF~4.7uF bypass capacitor in parallel needs to be added.
GND	1, 27, 34, 36, 37, 40, 41		Ground		

Reset Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESET	15	DI	Reset the module	R_{PU}≈78kΩ V_{IH}max=3.3V V_{IH}min=2.1V V_{IL}max=0.6V	Pulled up internally. Active low.
Network Status Indicator					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NETLIGHT	16	DO	Network status indication (Disable by default)	V_{OL}max=0.3V V_{OH}min=2.4V	3.0V power domain. If unused, keep this pin open.
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC*	9	AI	General-purpose analog to digital converter interface	Input voltage range: 0V to 4.0V	The maximum ADC input voltage should be lower than that of the VBAT voltage. If unused, keep this pin open.
UART Port					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RXD	18	DI	Receive data from TXD of DTE	V_{IL}max=0.6V V_{IH}min=2.1V V_{IH}max=3.3V	3.0V power domain. Cannot be left floating in PSM.
TXD	17	DO	Send data to RXD of DTE	V_{OL}max=0.3V V_{OH}min=2.4V	3.0V power domain.
RI	20	DO	Ring Indicator: the module will output signals to inform the DTE when an SMS message is received or data is transmitted	V_{OL}max=0.3V V_{OH}min=2.4V	3.0V power domain. If unused, keep this pin open.

Debug Port					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
DBG_RXD	38	DI	Receive data from the COM port of DTE	V_{IL}max=0.6V V_{IH}min=2.1V V_{IH}max=3.3V	3.0V power domain. If unused, keep this pin open.
DBG_TXD	39	DO	Send data to the COM port of DTE	V_{OL}max=0.3V V_{OH}min=2.4V	3.0V power domain. If unused, keep this pin open.
USIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_VDD	14	DO	Power supply for USIM card	Vnorm=1.8/3.0V	All signals of USIM interface should be protected against ESD with a TVS diode array. Maximum trace length from the module pad to USIM card connector is 200mm.
USIM_RST	12	DO	USIM card reset signal	V_{OL}max=0.1×USIM_VDD V_{OH}min=0.8×USIM_VDD	
USIM_DATA	11	IO	USIM card data signal	V_{OL}max=0.1×USIM_VDD V_{OH}min=0.8×USIM_VDD V_{IL}min=-0.1×USIM_VDD V_{IL}max=0.2×USIM_VDD V_{IH}min=0.7×USIM_VDD V_{IH}max=1.1×USIM_VDD	
USIM_CLK	13	DO	USIM card clock signal	V_{OL}max=0.1×USIM_VDD V_{OH}min=0.8×USIM_VDD	
USIM_GND	10		Specified ground for USIM card		
RF Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RF_ANT	35	IO	RF antenna pad		50Ω impedance
RESERVED Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	2~8, 19, 21, 22, 23, 25, 26, 28~33, 44~58		Reserved		Keep these pins unconnected.

NOTE

"*" means under development.

3.4. Operating Modes

There are three operating modes of BC68, which determines availability of functions at different power-saving levels.

Table 5: Overview of Operating Modes

Mode	Function	
Normal Operation	Active	In active mode, all functions of the module are available and all processors are active. Radio transmission and reception can be performed. Transitions to idle mode or PSM can be initiated in active mode.
	Idle	In Idle mode, the software is active when the module has registered on the network and is ready to send and receive data; paging messages can be received; transitions to active mode or PSM can be initiated in idle mode.
	PSM	In PSM, only the 32kHz RTC is active, the network is disconnected and paging messages cannot be received either. When MO (Mobile Originated) data are sent or the periodic TAU (Tracking Area Update) timer T3412 expires, the module will be woken up.

3.5. Power Saving Mode (PSM)

PSM is designed to reduce power consumption of the module and improve the battery life. The following figure shows the power consumption in different modes.

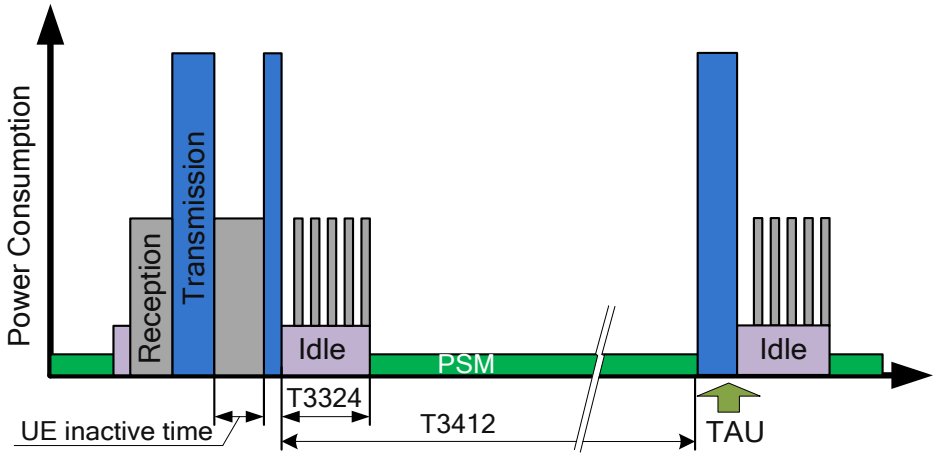


Figure 3: Module Power Consumption in Different Modes

The procedure of the module entering PSM is as follows:

The module requests to enter PSM through the “ATTACH REQUEST” message during attach/TAU (Tracking Area Update) procedure. Then the network accepts the request and provides an active time value (T3324) to the module, during which the mobile reachable timer starts. When the T3324 timer expires, the module enters PSM for duration of T3412 (periodic TAU timer). Please note that the module cannot request PSM when establishing emergency attachment or initializing PDN (Public Data Network) connection.

In PSM, BC68 cannot be paged and stops accessing to network activities such as cell reselection, while T3412 is still active.

There are two approaches for the module to exit PSM: DTE takes the initiative to send MO (Mobile Originated) data to quit PSM; or the periodic TAU timer expires, the module will exit PSM.

3.6. Power Supply

3.6.1. Power Supply Pins

BC68 provides two VBAT pins for the connection to an external power supply.

The following table shows VBAT pins and ground pins of the module.

Table 6: VBAT and GND Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT	42, 43	Power supply for the module	3.1	3.6	4.2	V
GND	1, 27, 34, 36, 37, 40, 41	Ground		0		V

3.6.2. Reference Design for Power Supply

The power design is vital to the module since the performance of the module largely depends on the power source. Power source for the module has to be capable of providing at least 0.5A.

A low quiescent current LDO can be applied as the power supply. Meanwhile, Li-SOCI2 batteries can also be used to supply power for the module. Power supply of the module ranges from 3.1V to 4.2V. Please ensure that the input voltage never drops below 3.1V even in burst transmission. If the power voltage drops below 3.1V, the module will not work normally.

For better power performance, it is recommended to place a 47uF tantalum capacitor with low ESR and three ceramic capacitors (100nF, 100pF and 22pF) near the VBAT pins, and to place a TVS diode on the VBAT trace to increase voltage surge withstand capability. WS4.5DPV is recommended (for more details about WS4.5DPV, please visit http://way-on.com/).

The following figure shows a reference circuit. In principle, the longer the VBAT trace is, the wider it should be.

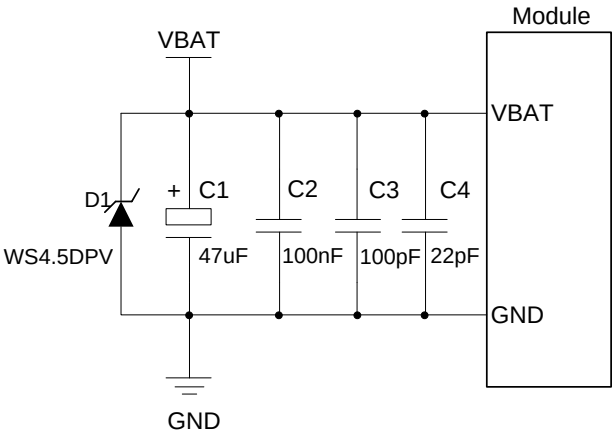


Figure 4: Reference Circuit for Power Supply

3.7. Turn on and off Scenarios

3.7.1. Turn on

The module can be automatically turned on by supplying power to VBAT pin with RESET signal not being pulled down.

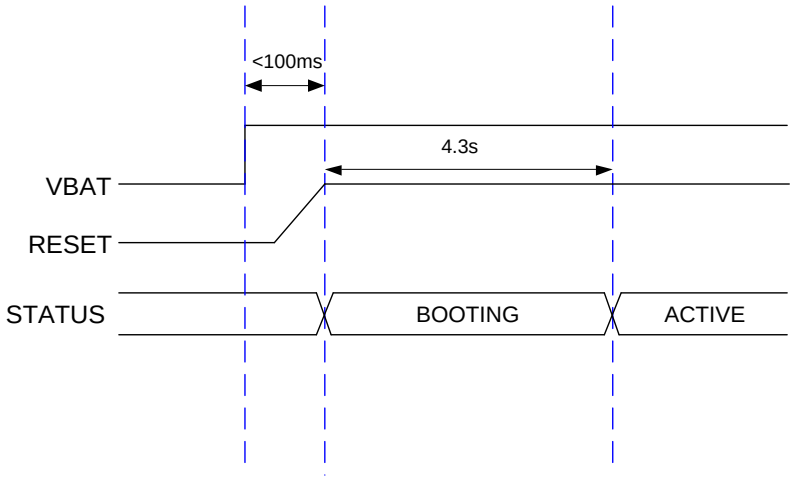


Figure 5: Turn-on Timing

NOTES

1. Due to internal pull-up, RESET will automatically change to high level after VBAT is powered up.
2. RESET signal cannot be pulled down during BOOTING.

3.7.2. Turn off

The module can be turned off by shutting down the VBAT power supply.

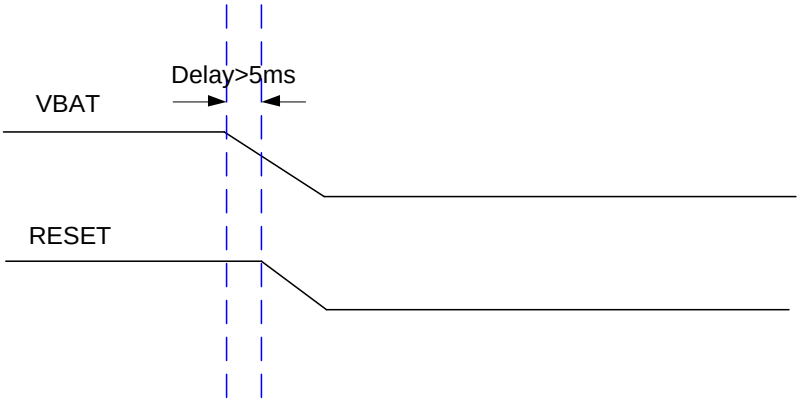


Figure 6: Turn-off Timing

3.7.3. Reset

The module can be reset through two ways:

- Hardware Reset: Reset the module by driving the reset pin to a low-level voltage for more than 100ms.
- Software Reset: Reset the module using command **AT+NRB**. For more details about the command, please refer to ***document [2]***.

Table 7: Reset Description

Pin Name	Pin No.	Description	Reset Pull-down Time
RESET	15	Reset the module. Active low.	>100ms

The recommended circuits of hardware reset are shown as below. An open drain/collector driver or button can be used to control the RESET pin.

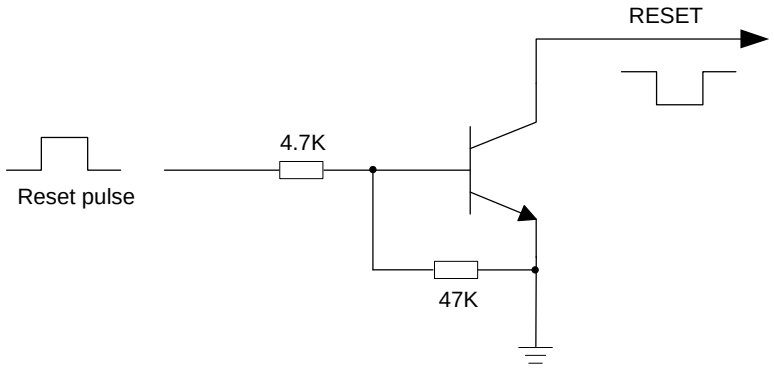


Figure 7: Reference Circuit of RESET with Driver Circuits

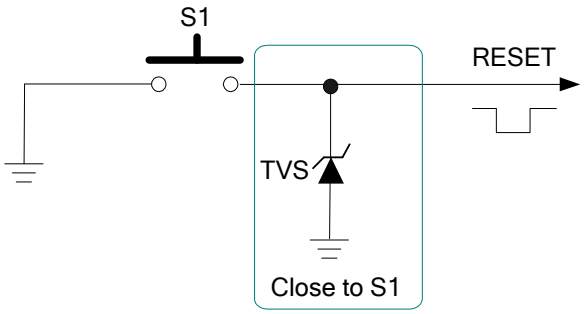


Figure 8: Reference Circuit of RESET with Buttons

3.8. UART Interfaces

The module provides two UART ports: main port and debug port. The module is designed as DCE (Data Communication Equipment), following the traditional DCE-DTE (Data Terminal Equipment) connection.

Table 8: Pin Definition of the UART Interfaces

Interfaces	Pin Name	Pin No.	Description	Comment
Main Port	RXD	18	Receive data from TXD of DTE	3.0V power domain
	TXD	17	Send data to RXD of DTE	
	RI	20	Ring Indicator: the module will output signals to inform DTE when an SMS message is received or data is transmitted	
Debug Port	DBG_RXD	38	Receive data from the COM port of DTE	
	DBG_TXD	39	Send data to the COM port of DTE	

The logic levels are described in the following table.

Table 9: Logic Levels of the UART Interfaces

Parameter	Min.	Max.	Unit
V_{IL}	-0.3	0.6	V
V_{IH}	2.1	3.3	V
V_{OL}		0.3	V
V_{OH}	2.4	3	V

Table 10: Main Port Settings

Parameter	Supported Value
Normal Mode Baud Rate	4800bps, 9600bps, 57600bps, 115200bps, 230400bps, 460800bps
PSM Baud Rate	4800bps, 9600bps, 57600bps

Download Baud Rate	115200bps, 921600bps
Parity	Even/Odd/None
Number of Stop Bits	1 or 2 bits
Data Bits Per Frame	8 bits

3.8.1. Main Port

The main port can be used for AT command communication and data transmission, and in such case the baud rate should be 4800bps, 9600bps (default), 57600bps, 115200bps, 230400bps and 460800bps. It can also be used for firmware upgrading, and in such case the baud rate should be 115200bps or 921600bps. The main port is available in active mode, idle mode and PSM. For more information about firmware upgrading, please refer to ***document [3]***.

The following figure shows the connection between the DCE and DTE.

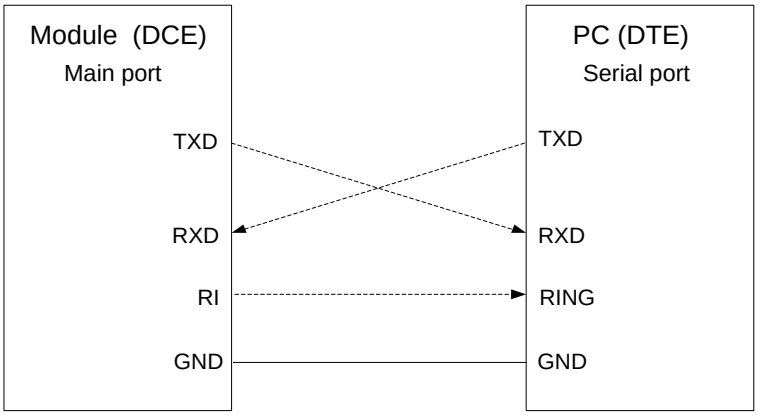


Figure 9: Reference Design for Main Port

3.8.2. Debug Port

The debug port is used to view log information with UEMonitor (a log viewer tool) for firmware debugging, and the baud rate is 921600bps. For detailed usage of UEMonitor, please refer to ***document [4]***.

A reference design for debug port is shown as below.

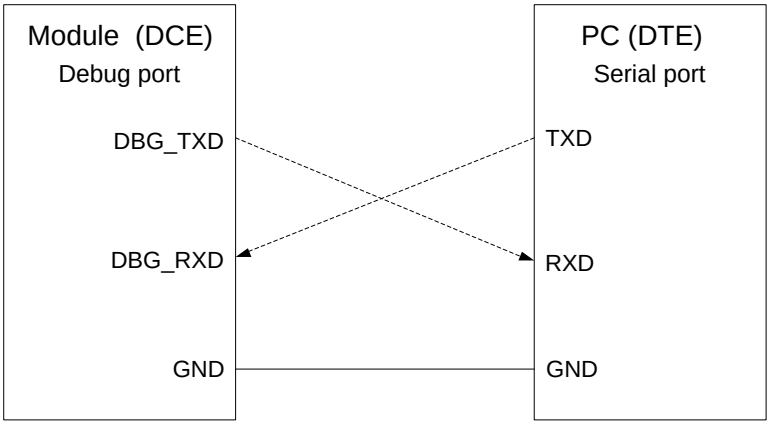


Figure 10: Reference Design for Debug Port

3.8.3. UART Application

A reference design of VCC level match is shown as below.

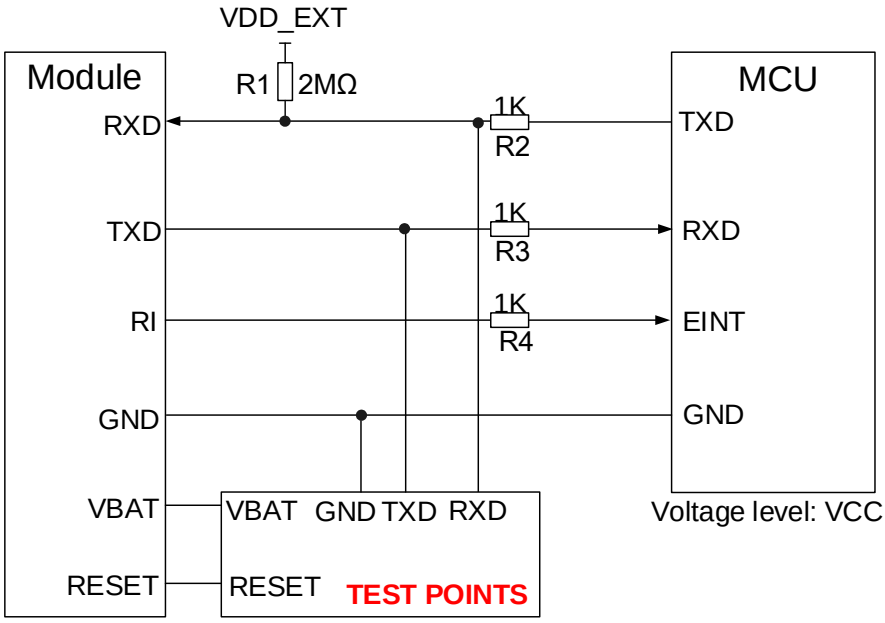


Figure 11: Level Match Design for VCC System

NOTES

1. In PSM, MCU_TXD cannot be left floating or the current consumption of BC68 in PSM will increase. It is recommended to connect a 2MΩ pull-up resistor (R1) between the module's RXD and VDD_EXT for low current consumption.
2. If VDD_EXT < VCC ≤ 3.6V, please change the pull-up resistor R1 to 20KΩ and change R2 to a Schottky diode (the cathode should be connected to MCU_TXD and the anode should be connected the module's RXD). Additionally, it is recommended to configure MCU_RXD as floating input in PSM (both pull-up and pull-down may cause current leakage when the module is in PSM).
3. If VCC < VDD_EXT or VCC > 3.6V, please use a triode or a low-turn-ON/OFF-delay-time MOSFET for level shift design to reduce the current leakage caused by I/O level mismatch.
4. It is recommended to reserve test points (of RXD, TXD, RESET and VBAT) for firmware upgrading.

The following circuit shows a reference design for the communication between the module and PC. Customers need to ensure level matching between devices.

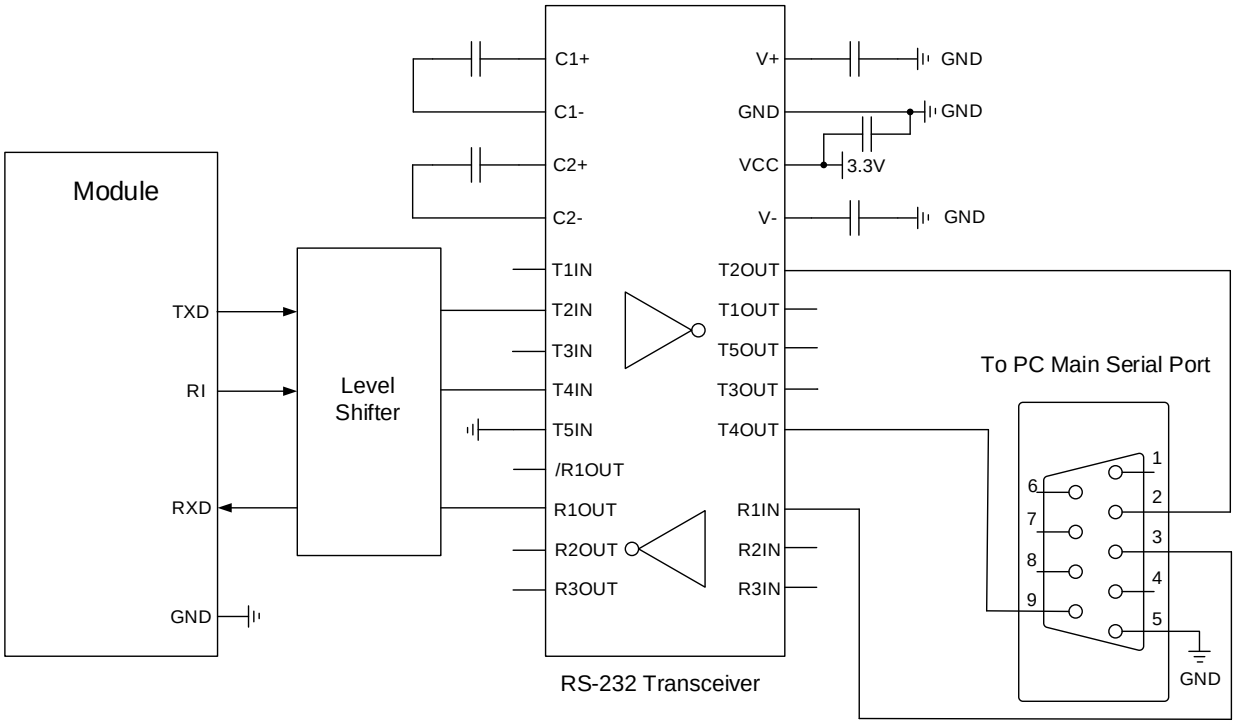


Figure 12: Sketch Map for RS-232 Interface Match

Please visit vendors' websites to select a suitable RS-232 transceiver IC, such as: http://www.exar.com and http://www.maximintegrated.com.

3.9. USIM Interface

The module provides one USIM interface allowing for access to external USIM cards. The interface supports the functionality of 3GPP specification and is intended to be used with a USIM application tool-kit.

The USIM interface is powered by an internal regulator in the module. Both 1.8V and 3.0V USIM cards are supported.

Table 11: PIN Definition of the USIM Interface

Pin Name	Pin No.	Description
USIM_VDD	14	Supply power for USIM card. USIM card voltage domain should be 1.8/3.0V±10%.
USIM_CLK	13	USIM card clock signal
USIM_DATA	11	USIM card data signal
USIM_RST	12	USIM card reset signal
USIM_GND	10	Specified ground for USIM card

A reference circuit of 6-pin USIM card connector is illustrated as the following figure.

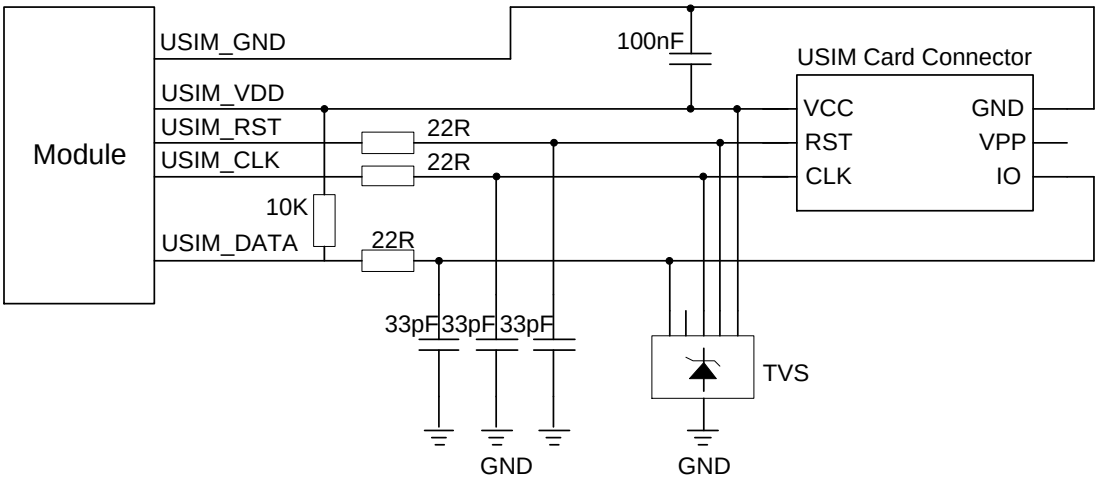


Figure 13: Reference Circuit of USIM Interface with 6-pin USIM Card Connector

For more information about USIM card connector, please visit http://www.amphenol.com and http://www.molex.com.

In order to guarantee reliability and availability of the USIM card in application, please follow the criteria below in USIM circuit design:

- Keep the USIM card connector as close to the module as possible and keep the trace length as less than 200mm as possible.
- Keep USIM card signals away from RF and VBAT traces.
- Assure trace between the ground of the module and that of the USIM card connector are short and wide. Trace width of ground needs to be no less than 0.5mm to maintain proper electric potential. The decouple capacitor of USIM_VDD is less than 1uF and must be placed near to USIM card connector.
- To avoid cross talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them separately with surrounded ground. USIM_RST should also be shielded with ground.
- In order to keep the module well-protected from ESD, it is recommended to add a TVS diode array. For more information about TVS diode, please visit http://www.onsemi.com. It is necessary to place the ESD protection device close to the USIM card connector and ensure that the USIM card signal trace from USIM card connector is connected to the ESD protection device first and then lead to the module. 22Ω resistors should be connected in series between the module and the USIM card connector so as to suppress EMI and enhance ESD protection. Please note that the peripheral USIM circuit should be close to the USIM card connector.
- Place the RF bypass capacitors (33pF) close to the USIM card connector on all signals traces to improve EMI suppression.

3.10. ADC Interface*

The module provides a 10-bit ADC input channel to read the voltage value. This ADC interface is available in both active and idle modes.

Table 12: Pin Definition of ADC

Pin Name	Pin No.	Description
ADC*	9	Analog to digital converter interface

NOTE

"*" means under development.

3.11. RI Behaviors

When an SMS message is received or certain URCs are reported, RI pin will be triggered. The behaviors of RI are shown as below.

Table 13: RI Behaviors

State	RI Response
Idle	HIGH
SMS	When an SMS message is received, the RI will turn to low level and stay for at least 120ms. The period depends on the length of output data and the baud rate.
URC	Certain URCs will trigger RI to turn into low level and stay for at least 120ms. The period depends on the length of output data and the baud rate.

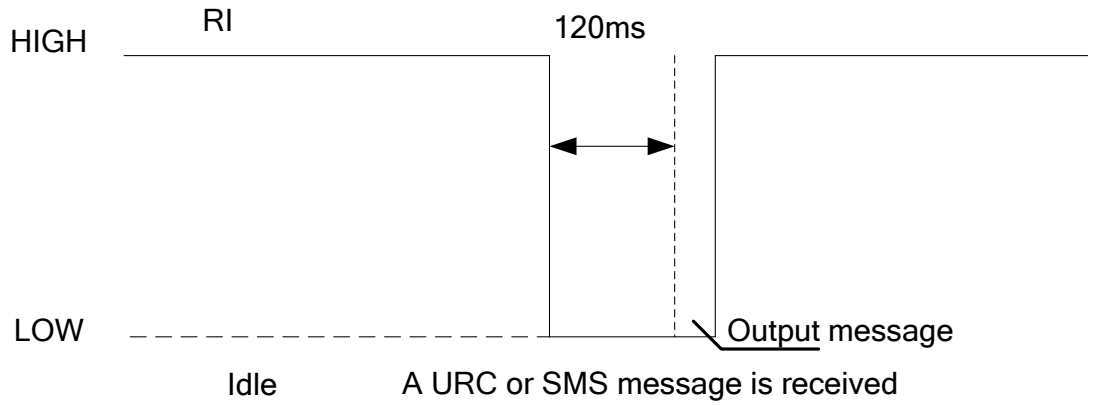


Figure 14: Behaviors of RI When a URC or SMS Message is Received

NOTE

When receiving SMS or URC information reports, the RI will output at low level for 120ms, and then output the data. The maximum time in which RI stays at low level depends on the length of URC data and the baud rate of the UART port.

3.12. Network Status Indication

This function is disabled by default and NETLIGHT pin outputs a low level. The function is enabled by the AT command **AT+QLEDMODE=1**, after which the NETLIGHT pin will work in states shown in the

following table.

Table 14: Working State of NETLIGHT

State	Module Function
64ms High (light on) / 800ms Low (light off)	The module is searching for network.
64ms High (light on) / 2000ms Low (light off)	The module is attached to network with connected status.
Low (light off)	Other status.

A reference circuit is shown as below.

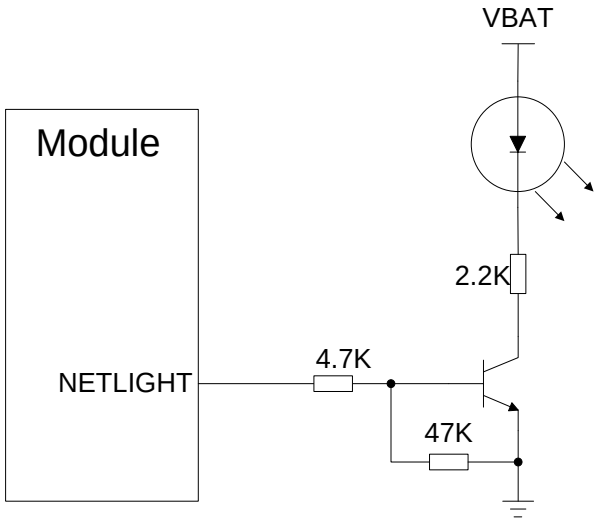


Figure 15: Reference Design for NETLIGHT

4 Antenna Interface

Pin 35 is for RF antenna. The RF antenna port has an impedance of 50Ω.

Table 15: Pin Definition of the RF Antenna Interface

Pin Name	Pin No.	Description
RF_ANT	35	RF antenna pad
GND	34, 36, 37	Ground

4.1. Reference Design of RF Antenna

A reference design of RF antenna is shown as below.

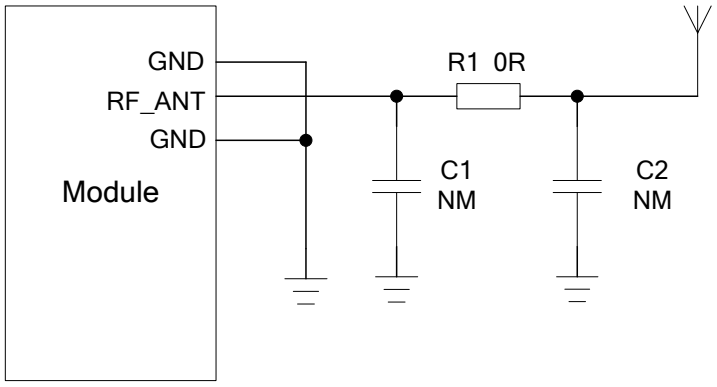


Figure 16: Reference Design of RF Antenna

BC68 provides an RF antenna pad for antenna connection. There are ground pads on each side of the antenna pad in order to guarantee a better grounding. Additionally, a π type matching circuit is recommended to adjust the RF performance. Please place the π-type matching components (R1/C1/C2) as close to the antenna as possible, and mount them according to practical needs. The capacitors (C1/C2) are not mounted and a 0Ω resistor is mounted on R1 by default.

4.2. Reference Design of RF Layout

For user's PCB, the characteristic impedance of all RF traces should be controlled to 50Ω. The impedance of a RF trace is usually determined by the trace width (W), the materials' dielectric constant, height from the reference ground to the signal layer (H), and the space between the RF trace and the ground (S). Microstrip and coplanar waveguide are typically used in RF layout to control characteristic impedance. The following figures are reference designs of microstrip or coplanar waveguide with different PCB structures.

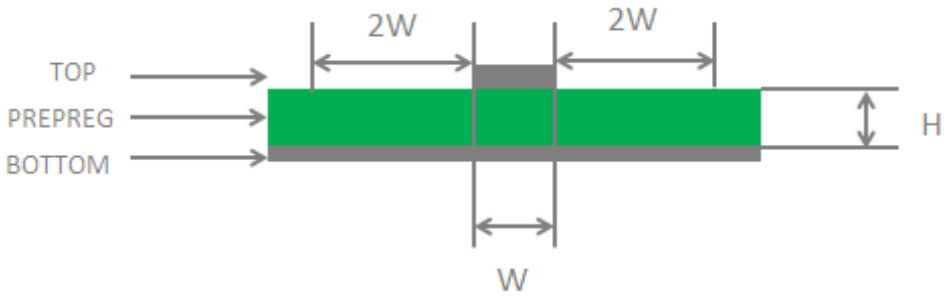


Figure 17: Microstrip Design on a 2-layer PCB

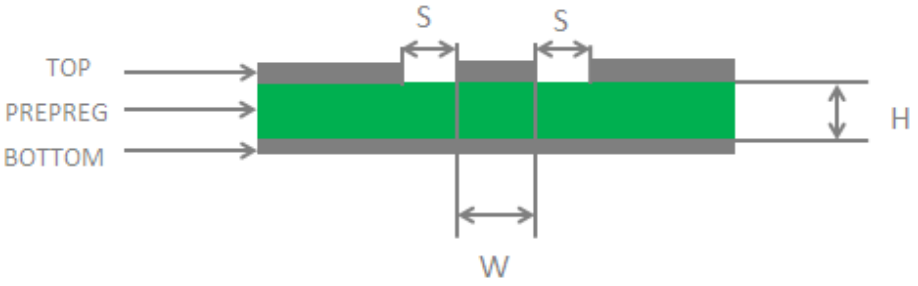


Figure 18: Coplanar Waveguide Design on a 2-layer PCB

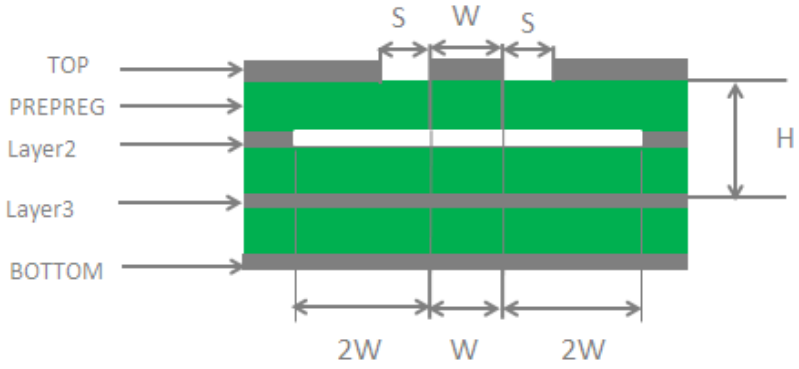


Figure 19: Coplanar Waveguide Design on a 4-layer PCB (Layer 3 as Reference Ground)

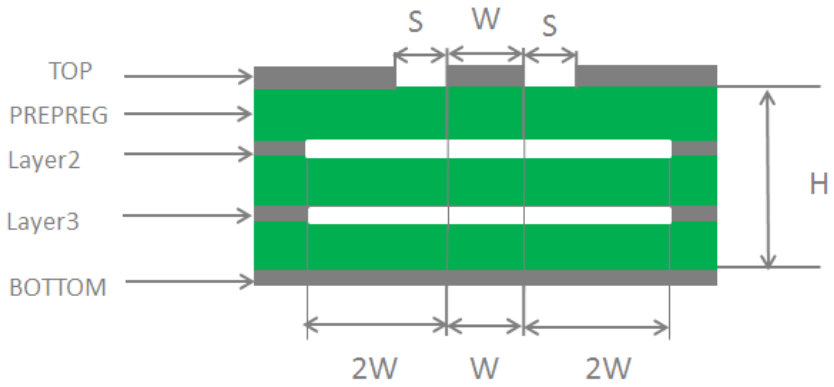


Figure 20: Coplanar Waveguide Design on a 4-layer PCB (Layer 4 as Reference Ground)

In order to ensure RF's performance and reliability, the following principles should be complied with in RF layout design:

- Use impedance simulation tool to accurately control the characteristic impedance of RF traces to 50Ω.
- The GND pins adjacent to RF pins should not be designed with thermal relief pads and should be fully connected to the ground.
- The distance between the RF pins and the RF connector should be as short as possible, and all the right-angle traces should be changed to curved ones. 135° angle is recommended.
- There should be a clearance between the signal pin and ground of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground will help to improve RF performance. The distance between the ground vias and RF traces should be over two times wider than the width of RF signal traces (2*W).

For more details about RF layout, please refer to ***document [5]***.

4.3. RF Output Power

Table 16: RF Output Power (Uplink QPSK and BPSK Modulation)

Frequency Band	Max.	Min.
Band 1	23dBm±2dB	<-40dBm
Band 3	23dBm±2dB	<-40dBm
Band 8	23dBm±2dB	<-40dBm

Band 5	23dBm±2dB	<-40dBm
Band 20	23dBm±2dB	<-40dBm
Band 28	23dBm±2dB	<-40dBm

NOTE

The design is compliant with the NB-IoT radio protocol in *3GPP Rel.14*.

4.4. RF Receiving Sensitivity

Table 17: RF Receiving Sensitivity without Retransmission (Throughput ≥ 95%)

Frequency Band	Receiving Sensitivity	3GPP
Band 1	-112dBm	-107.5dBm
Band 3	-112dBm	-107.5dBm
Band 8	-114dBm	-107.5dBm
Band 5	-114dBm	-107.5dBm
Band 20	-114dBm	-107.5dBm
Band 28	-114dBm	-107.5dBm

Table 18: RF Receiving Sensitivity in 128 Retransmissions (Throughput ≥ 95%)

Frequency Band	Receiving Sensitivity
Band 1	-128dBm
Band 3	-128dBm
Band 8	-130dBm
Band 5	-130dBm
Band 20	-130dBm
Band 28	-130dBm

4.5. Operating Frequency

Table 19: Operating Frequency

Frequency Band	Receiving Frequency	Transmitting Frequency
Band 1	2110MHz~2170MHz	1920MHz~1980MHz
Band 3	1805MHz~1880MHz	1710MHz~1785MHz
Band 8	925MHz~960MHz	880MHz~915MHz
Band 5	869MHz~894MHz	824MHz~849MHz
Band 20	791MHz~821MHz	832MHz~862MHz
Band 28	758MHz~803MHz	703MHz~748MHz

4.6. Antenna Requirements

The following table exhibits requirements for parameters of NB-IoT antenna.

Table 20: Antenna Cable Insertion Loss Requirements

Frequency Range	Requirement
703MHz~960MHz	Insertion Loss: <1dB
1710MHz~2200MHz	Insertion Loss: <1dB

Table 21: Antenna Parameter Requirements

Parameters	Requirements
Frequency Range	703MHz~960MHz; 1710MHz~2200MHz
VSWR	≤2
Gain (dBi)	≥1
Maximum Input Power (W)	50
Input Impedance (Ω)	50
Polarization Type	Linear

4.7. Recommended RF Connector for Antenna Installation

If RF connector is used for antenna connection, it is recommended to use U.FL-R-SMT connector provided by HIROSE.

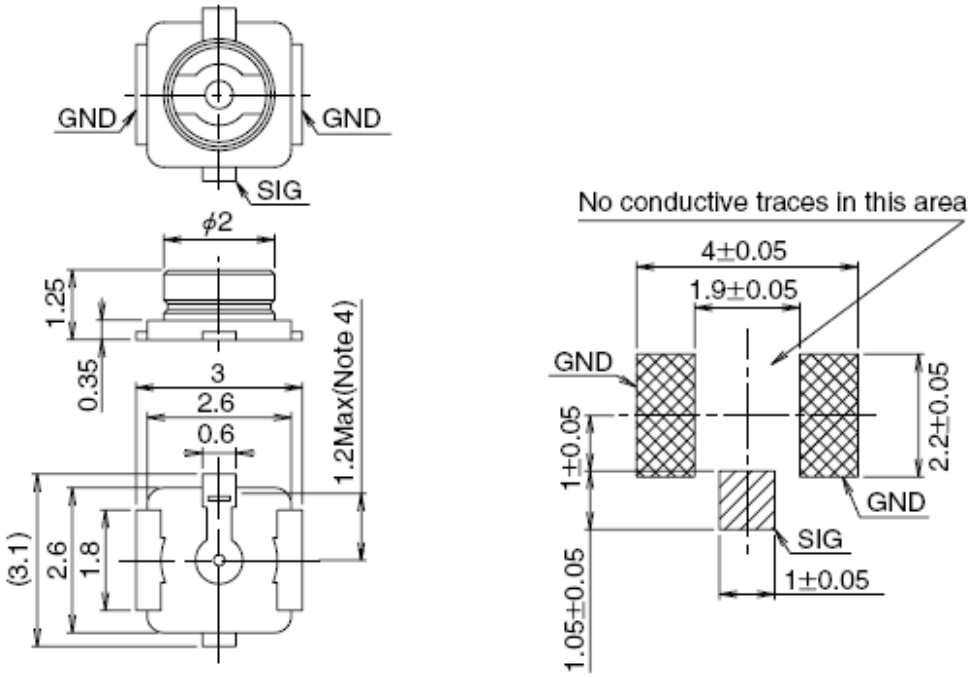


Figure 21: Dimensions of the U.FL-R-SMT Connector (Unit: mm)

U.FL-LP series connector listed in the following figure can be used to match the U.FL-R-SMT.

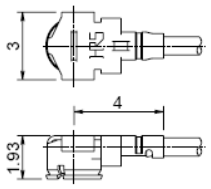
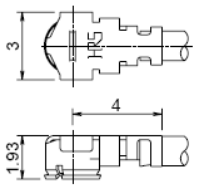
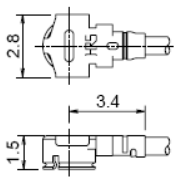
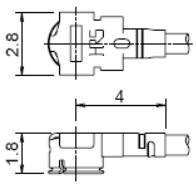
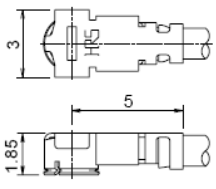
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 22: Mechanicals of U.FL-LP Connectors

The following figure describes the space factor of mated connector.

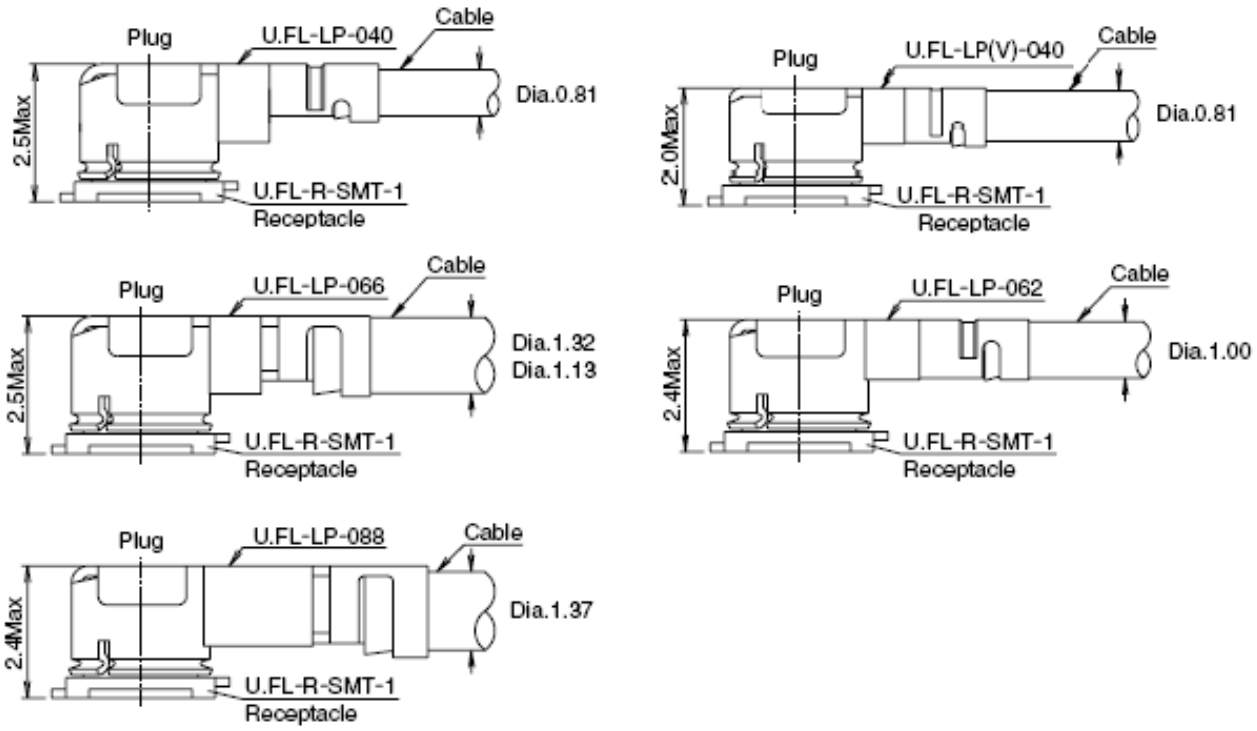


Figure 23: Space Factor of Mated Connector (Unit: mm)

For more details, please visit http://www.hirose.com.

5 Electrical, Reliability and Radio Characteristics

5.1. Absolute Maximum Ratings

Absolute maximum ratings of voltage on the module's digital and analog pins are listed in the following table.

Table 22: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.3	+4.25	V
Voltage at Digital Pins	-0.3	+4.25	V
Voltage at Analog Pins	-0.3	+4.25	V
Voltage at Digital/Analog Pins in Power-off Mode	-0.25	+0.25	V

5.2. Operation and Storage Temperatures

Table 23: Operation and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operation Temperature Range [1)]	-35	+25	+75	ºC
Extended Temperature Range [2)]	-40		+85	ºC
Storage Temperature Range	-40		+90	ºC

NOTES

1. [1] Within operation temperature range, the module meets 3GPP specification.
2. [2] Within extended temperature range, the module remains the ability to establish and maintain a SMS, data transmission, etc. and there is no unrecoverable malfunction. There is also no effect on radio spectrum and no harm to radio network. Only few parameters like P_{out} might reduce in their value and exceed specified tolerances. When the temperature returns to the operation temperature level, the module will comply with 3GPP specifications again.

5.3. Current Consumption

The values of current consumption are shown below.

Table 24: Current Consumption

Parameter	Description	Conditions	Min.	Typ.	Max.	Unit
I_{VBAT}	PSM	Deep sleep state		3		uA
	Idle mode	Standby state, DRX=2.56s, ECL0		0.5		mA
	Active mode @Single-tone (3.75kHz/15kHz)	Radio transmission, 23dBm (B1/B3)		250		mA
		Radio transmission, 23dBm (B8/B5/B20)		220		mA
		Radio transmission, 23dBm (B28)		280		mA
		Radio transmission, 12dBm (B1/B3/B8/B5/B20/B28)		130		mA
		Radio transmission, 0dBm (B1/B3/B8/B5/B20/B28)		70		mA
		Radio reception		60		mA
	Active mode @Multi-tone (15kHz)	Radio transmission, 23dBm (B1/B3/B8/B5/B20/B28)		350		mA

5.4. Electrostatic Discharge

The module is not protected against electrostatic discharge (ESD) in general. Consequently, it is important to refer to ESD handling precautions when applying ESD sensitive components. Proper ESD handling and packaging procedures must be applied throughout the processing, handling, operation any application that incorporates the module.

The following table shows the module's electrostatic discharge characteristics at temperature of 25°C and relative humidity of 45%.

Table 25: Electrostatic Discharge Characteristics

Test Points	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna Interface	±5	±10	kV
Other Interfaces	±0.5	±1	kV

6 Mechanical Dimensions

This chapter describes the mechanical dimensions of the module. All dimensions are measured in mm. The tolerances for dimensions without tolerance values are ±0.05mm.

6.1. Mechanical Dimensions of the Module

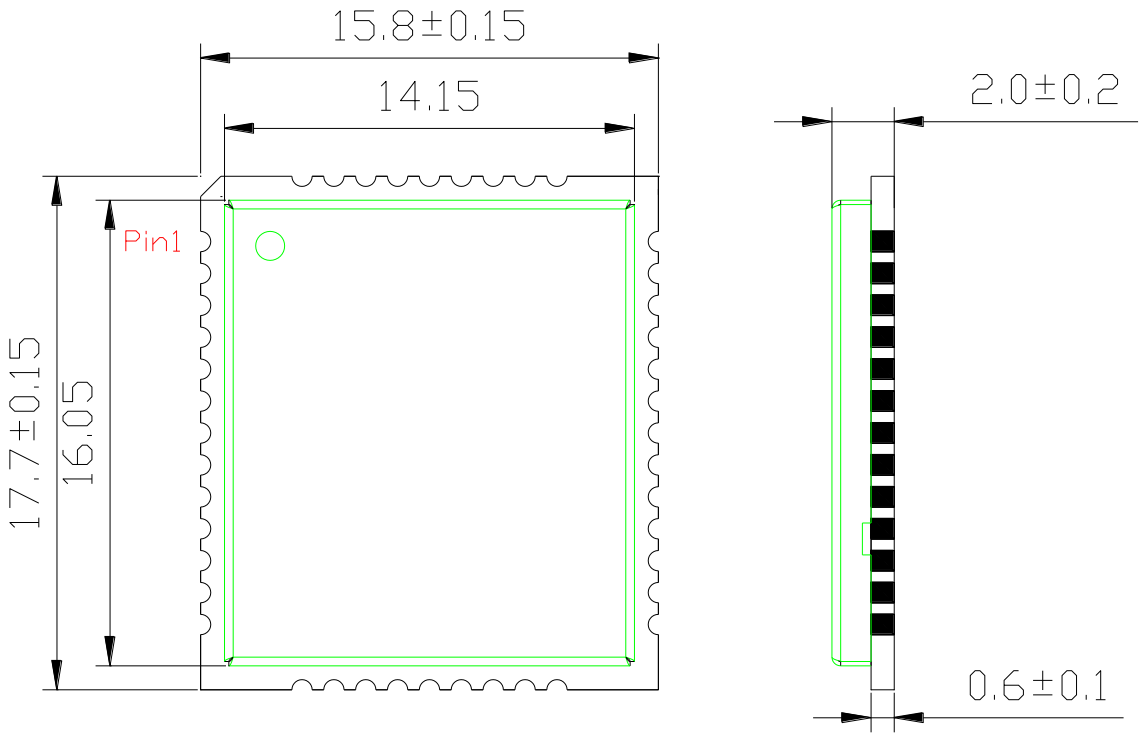


Figure 24: Top and Side Dimensions

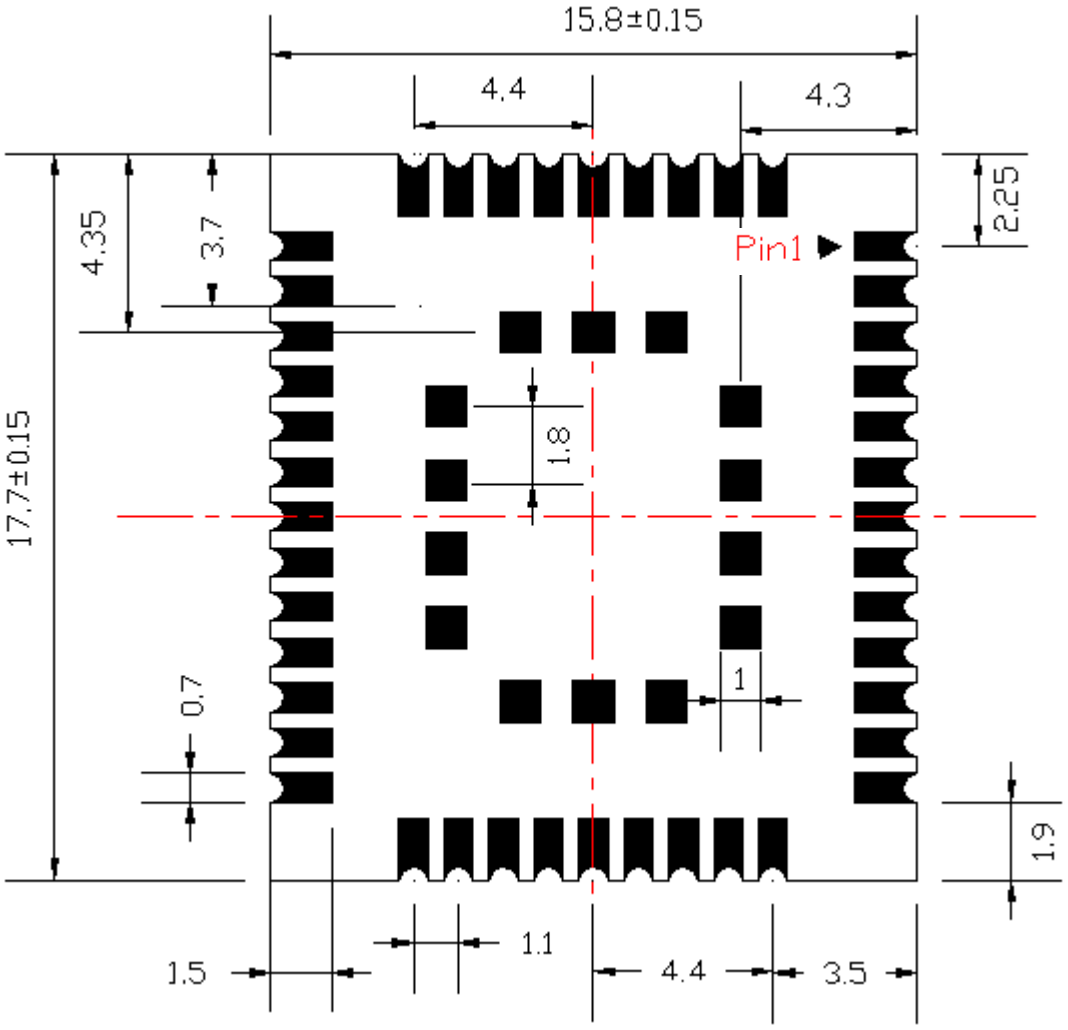


Figure 25: Bottom Dimensions (Bottom View)

6.2. Recommended Footprint

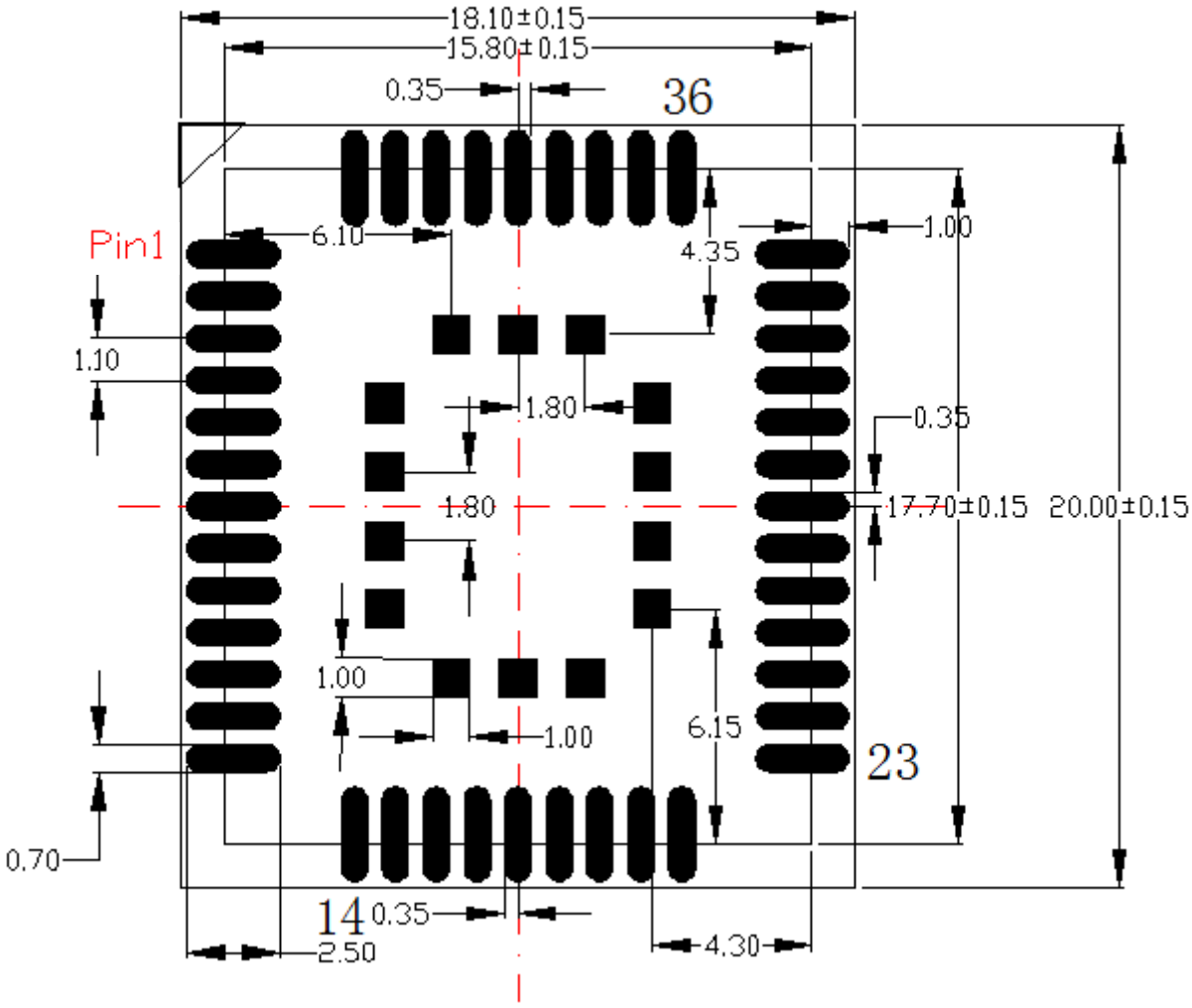


Figure 26: Recommended Footprint (Top View)

NOTES

1. For easy maintenance of the module, please keep a distance of no less than 3mm between the module and other components on host boards.
2. All RESERVED pins must not be connected to GND.

6.3. Top and Bottom Views of the Module

Figure 27: Top View of the Module

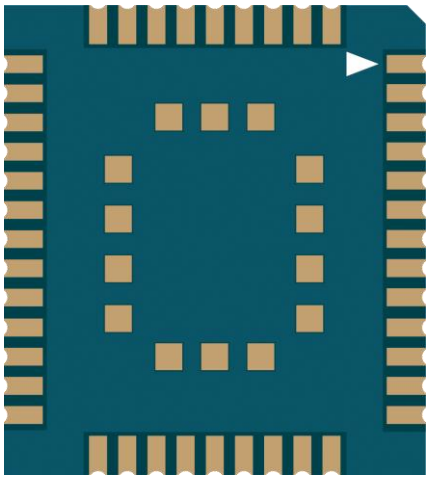


Figure 28: Bottom View of the Module

NOTE

These are renderings of BC68. For authentic dimension and appearance, please refer to the module that you receive from Quectel.

7 Storage, Manufacturing and Packaging

7.1. Storage

BC68 module is stored in a vacuum-sealed bag. It is rated at MSL 3, and its storage restrictions are shown as below.

1. Shelf life in the vacuum-sealed bag: 12 months at <40ºC/90%RH.

2. After the vacuum-sealed bag is opened, devices that will be subjected to reflow soldering or other high temperature processes must be:
   - Mounted within 168 hours at the factory environment of ≤30ºC/60%RH.
   - Stored at <10%RH.

3. Devices require baking before mounting, if any circumstance below occurs.
   - When the ambient temperature is 23ºC±5ºC and the humidity indication card shows the humidity is >10% before opening the vacuum-sealed bag.
   - Device mounting cannot be finished within 168 hours at factory conditions of ≤30ºC/60%.

4. If baking is required, devices may be baked for 8 hours at 120ºC±5ºC.

NOTE

As the plastic package cannot be subjected to high temperature, it should be removed from devices before high temperature (120ºC) baking. If shorter baking time is desired, please refer to the *IPC/JEDECJ-STD-033* for baking procedure.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. The force on the squeegee should be adjusted properly

to produce a clean stencil surface on a single pass. To ensure the module soldering quality, the thickness of stencil for the module is recommended to be 0.18mm~0.20mm. For more details, please refer to ***document [6]***.

It is suggested that the peak reflow temperature is 238~245ºC, and the absolute maximum reflow temperature is 245ºC. To avoid damage to the module caused by repeated heating, it is strongly recommended that the module should be mounted after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

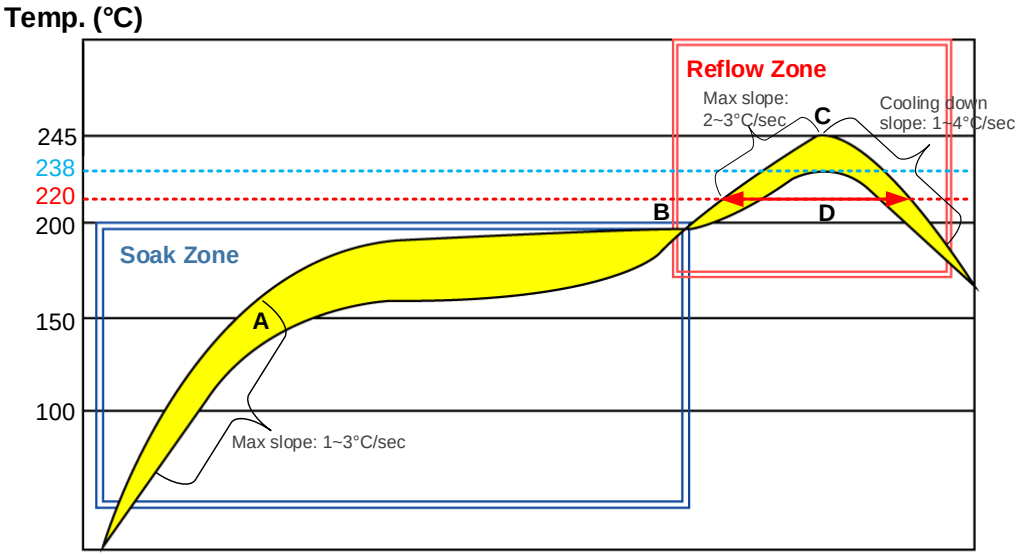


Figure 29: Reflow Soldering Thermal Profile

Table 26: Recommended Thermal Profile Parameters

Factor	Recommendation
Soak Zone	
Max slope	1 to 3°C/sec
Soak time (between A and B: 150°C and 200°C)	60 to 120 sec
Reflow Zone	
Max slope	2 to 3°C/sec
Reflow time (D: over 220°C)	40 to 60 sec
Max temperature	238°C ~ 245°C
Cooling down slope	1 to 4°C/sec

Reflow Cycle	
Max reflow cycle	1

NOTES

1. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
2. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.

7.3. Packaging

The modules are stored inside a vacuum-sealed bag which is ESD protected. It should not be opened until the devices are ready to be soldered onto the application.

7.3.1. Tape and Reel Packaging

The reel is 330mm in diameter and each reel contains 250 modules.

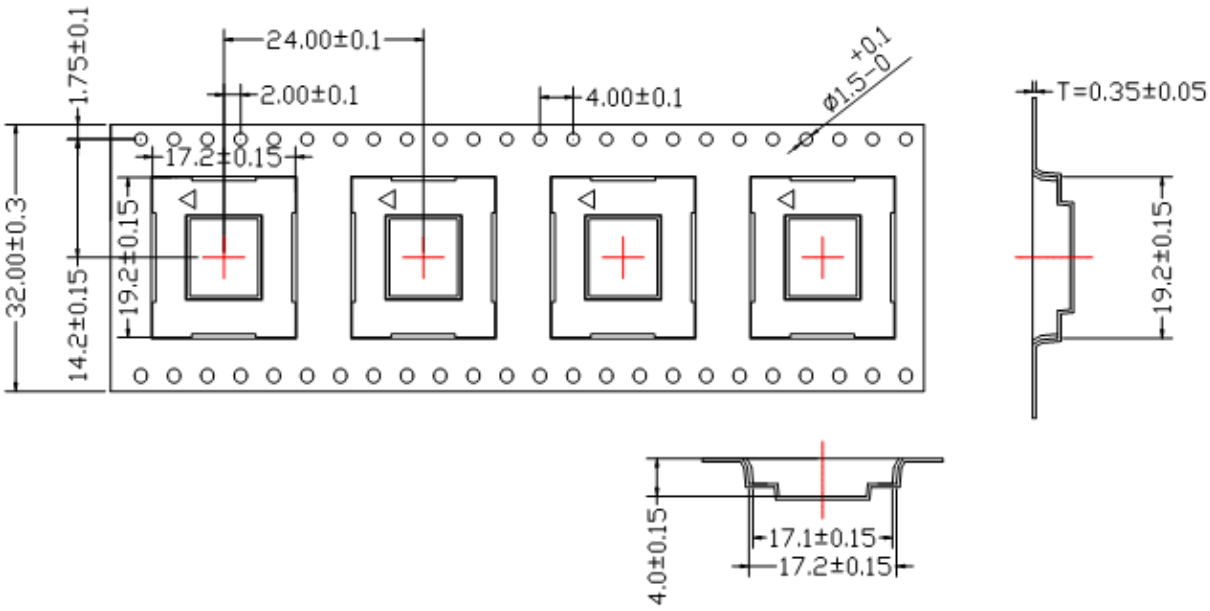


Figure 30: Tape Dimensions (Unit)

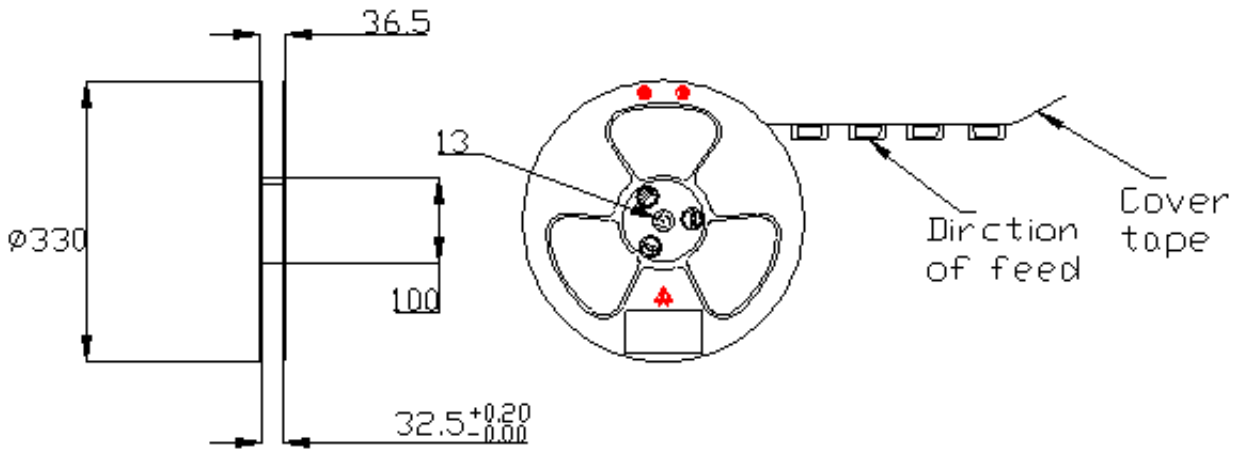


Figure 31: Reel Dimensions (Unit)

8 Appendix A References

Table 27: Related Documents

SN	Document Name	Remark
[1]	Quectel_BC68-TE-B_User_Guide	BC68-TE-B User Guide
[2]	Quectel_BC95-G&BC68_AT_Commands_Manual	AT Commands Manual for BC68 and BC95-G
[3]	Quectel_BC95-G&BC68_Firmware_Upgrade_User_Guide	Firmware Upgrade User Guide for BC68 and BC95-G
[4]	Quectel_BC95-G&BC68_UEMonitor_User_Guide	UEMonitor User Guide for BC68 and BC95-G
[5]	Quectel_RF_Layout_Application_Note	RF Layout Application Note
[6]	Quectel_Module_Secondary_SMT_User_Guide	Module Secondary SMT User Guide

Table 28: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
DCE	Data Communications Equipment (typically module)
DTE	Data Terminal Equipment (typically computer, external controller)
DRX	Discontinuous Reception
H-FDD	Half Frequency Division Duplexing
I/O	Input/Output
IC	Integrated Circuit
Imax	Maximum Load Current
Inorm	Normal Current

kbps	Kilo Bits Per Second
LED	Light Emitting Diode
MO	Mobile Originated
MT	Mobile Terminated
NB-IoT	Narrow Band Internet of Things
PCB	Printed Circuit Board
PDN	Public Data Network
PSM	Power Saving Mode
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
RTC	Real Time Clock
USIM	Universal Subscriber Identification Module
SMS	Short Message Service
TAU	Tracking Area Update
UART	Universal Asynchronous Receiver & Transmitter
URC	Unsolicited Result Code
VSWR	Voltage Standing Wave Ratio
Vmax	Maximum Voltage Value
Vnorm	Normal Voltage Value
Vmin	Minimum Voltage Value
$V_{IH}max$	Maximum Input High Level Voltage Value
$V_{IH}min$	Minimum Input High Level Voltage Value
$V_{IL}max$	Maximum Input Low Level Voltage Value
$V_{IL}min$	Minimum Input Low Level Voltage Value
$V_{I}max$	Absolute Maximum Input Voltage Value

$V_I$min	Absolute Minimum Input Voltage Value
V_{OH}max	Maximum Output High Level Voltage Value
V_{OH}min	Minimum Output High Level Voltage Value
V_{OL}max	Maximum Output Low Level Voltage Value
V_{OL}min	Minimum Output Low Level Voltage Value