BC660K-GL

Hardware Design

NB-IoT Module Series

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Safety Information

The following safety precautions must be observed during all phases of operation, such as usage, service or repair of any cellular terminal or mobile incorporating the module. Manufacturers of the cellular terminal should notify users and operating personnel of the following safety information by incorporating these guidelines into all manuals of the product. Otherwise, Quectel assumes no liability for customers' failure to comply with these precautions.

Full attention must be paid to driving at all times in order to reduce the risk of an accident. Using a mobile while driving (even with a handsfree kit) causes distraction and can lead to an accident. Please comply with laws and regulations restricting the use of wireless devices while driving.

Switch off the cellular terminal or mobile before boarding an aircraft. The operation of wireless appliances in an aircraft is forbidden to prevent interference with communication systems. If there is an Airplane Mode, it should be enabled prior to boarding an aircraft. Please consult the airline staff for more restrictions on the use of wireless devices on an aircraft.

Wireless devices may cause interference on sensitive medical equipment, so please be aware of the restrictions on the use of wireless devices when in hospitals, clinics or other healthcare facilities.

Cellular terminals or mobiles operating over radio signal and cellular network cannot be guaranteed to connect in certain conditions, such as when the mobile bill is unpaid or the (U)SIM card is invalid. When emergency help is needed in such conditions, use emergency call if the device supports it. In order to make or receive a call, the cellular terminal or mobile must be switched on in a service area with adequate cellular signal strength. In an emergency, the device with emergency call function cannot be used as the only contact method considering network connection cannot be guaranteed under all circumstances.

The cellular terminal or mobile contains a transceiver. When it is ON, it receives and transmits radio frequency signals. RF interference can occur if it is used close to TV sets, radios, computers or other electric equipment.

In locations with explosive or potentially explosive atmospheres, obey all posted signs and turn off wireless devices such as mobile phone or other cellular terminals. Areas with explosive or potentially explosive atmospheres include fueling areas, below decks on boats, fuel or chemical transfer or storage facilities, and areas where the air contains chemicals or particles such as grain, dust or metal powders.

About the Document

Revision History

Version	Date	Author	Description
-	2020-09-30	Clifton HE/ Ellison WANG/ Randy LI	Creation of the document
1.0	2021-01-12	Clifton HE/ Ellison WANG/ Randy LI	First official release
1.1	2021-06-03	Clifton HE/ Ellison WANG/ Randy LI	1. Deleted the relevant part of B14. 2. Chapter 1: Added table 1. 3. Chapter 2.2: Updated the status of MQTT protocol. 4. Chapter 5.1: Added this section. 5. Chapter 7.1 and 7.2: Updated the requirements on storage, manufacturing and soldering.
1.2	2022-09-09	Winks WANG/ Ellison WANG/ Randy LI	1. Deleted PDU mode in SMS feature (Table 3). 2. Added the load current of DC characteristics for VDD_EXT (Table 5). 3. Added information about ultrasonic cleaning (Chapter 7.2).
1.3	2023-06-02	Weida LIU/ Hugh ZHANG/ Yance YANG	1. Added the network protocols CoAP, CoAPS, HTTP and HTTPS (Table 2). 2. Updated the output power supply (VDD_EXT) from 1.8/3.3 V to 1.8 V/3.1–3.3 V. 3. Added TVS selection parameter requirements (Table 9). 4. Added voltage stability requirements (Chapter 3.5.2). 5. Added the truth table of GRFC interfaces (Table 20). 6. Updated the recommended reflow soldering

	thermal profile and the relevant parameters. (Figure 32 and Table 34). 7. Updated the recommended reflow soldering thermal profile and the relevant parameters. (Figure 32 and Table 34).

Contents

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1 Introduction

This document defines BC660K-GL and describes its air interface and hardware interfaces which are connected with your applications.

With this document, you can quickly understand module interface specifications, electrical and mechanical details, as well as other related information of the module. The document, coupled with application notes and user guides, makes it easy to design and set up mobile applications with the module.

2 Product Overview

2.1. Frequency Bands and Functions

BC660K-GL is a high-performance NB-IoT module with extremely low power consumption. It is designed to communicate with infrastructures of mobile network operators through NB-IoT radio protocols supported by 3GPP Rel-13 and Rel-14. BC660K-GL supports a broad range of frequency bands as listed below.

Table 1: Frequency Bands of BC660K-GL

Mode	Frequency Bands
LTE HD-FDD	B1/B2/B3/B4/B5/B8/B12/B13/B17/B18/B19/B20/B25/B28/B66/B70/B85

BC660K-GL is an SMD type module with LCC and LGA package, and has an ultra-compact profile of 17.7 mm × 15.8 mm × 2.0 mm, which makes it easily embedded into size-constrained applications and provide reliable connectivity with the applications.

BC660K-GL provides abundant external interfaces (UART, ADC, USIM, etc.) and protocol stacks (UDP/TCP/LwM2M/MQTT, etc.), which facilitate the module's application.

The module's compact form factor, ultra-low power consumption and extended temperature range make it one of the best choices for a wide range of IoT application, such as smart metering, bike sharing, smart wearables, smart parking, smart city, home appliances, security and asset tracking, agricultural and environmental monitoring, etc. It also provides a complete range of SMS and data transmission services to meet various user demands.

2.2. Key Features

The following table describes the detailed features of BC660K-GL.

Table 2: Key Features

Feature	Details
Power Supply	**VBAT:** ● Supply voltage: 2.2–4.3 V ● Typical supply voltage: 3.3 V
Power Saving	Typical power consumption (in Deep Sleep mode): 800 nA
Frequency Bands	**LTE Cat NB2:** B1/B2/B3/B4/B5/B8/B12/B13/B17/B18/B19/B20/B25/B28/B66/B70/B85
Transmitting Power	23 dBm ±2.7 dB
eSIM [1]	Reserved with 2.552 × 2.722 mm package
UART	**Main UART:** ● Used for AT command communication and data transmission, where the baud rate is 115200 bps by default. For more details, see ***Chapter 3.7.1*** ● Used for firmware upgrade, where the baud rate is 921600 bps by default. **Debug UART:** ● Used for software debugging ● Default baud rate: 6 Mbps
USIM Interface	Supports 1.8/3.0 V USIM card
Network Protocols	UDP/TCP/PING/LwM2M/SNTP/MQTT/MQTTS/SSL/TLS/CoAP/CoAPS/ HTTP/HTTPS
SMS	Text Mode
Data Transmission Features	● Single-tone (max.): 25.5 kbps (DL)/16.7 kbps (UL) ● Multi-tone (max.): 127 kbps (DL)/158.5 kbps (UL)
AT Commands	● *3GPP TS 27.005/3GPP TS 27.007* AT commands (3GPP Rel-13) ● Quectel enhanced AT commands
Firmware Update	● Upgrade firmware via main UART ● Upgrade firmware via DFOTA
Real Time Clock	Supported
Physical Characteristics	● Size: (17.7 ±0.15) mm × (15.8 ±0.15) mm × (2.0 ±0.2) mm

[1] eSIM is reserved and not included by default.

	• Weight: 1.0 ±0.2 g
Temperature Range	• Operating temperature range: -35 to +75 °C [2] • Extended temperature range: -40 to +85 °C [3] • Storage temperature range: -40 to +90 °C
Antenna Interface	50 Ω impedance
RoHS	All hardware components are fully compliant with EU RoHS directive

2.3. Functional Diagram

The following figure shows a block diagram of BC660K-GL and illustrates the major functional parts.

- RF Transceiver and Subsystem
- Baseband
- Power Management Unit
- Peripheral Interfaces

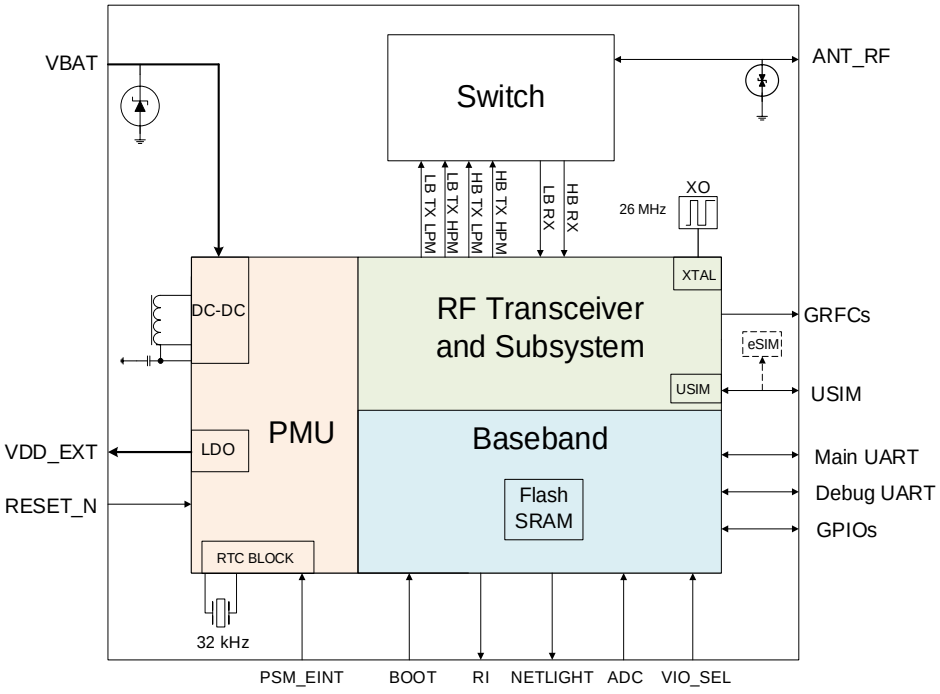


Figure 1: Functional Diagram

2 Within the operating temperature range, the module meets 3GPP specifications.
3 Within the extended temperature range, the module remains the ability to establish and maintain functions such as SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

2.4. TE-B Kit

Quectel supplies an evaluation board (BC660K-GL-TE-B) with accessories to control or test the module. For more details, see ***document [1]***.

3 Application Functions and Interfaces

BC660K-GL is equipped with 58 pins, including 44 LCC pins and 14 LGA pins. The subsequent chapters provide detailed descriptions of the following functions/pins/interfaces:

- Power Supply
- PSM_EINT
- RESET_N
- BOOT
- UART
- USIM Interface
- ADC Interface
- RI
- GPIO interfaces
- GRFC interfaces
- NETLIGHT

3.1. Pin Assignment

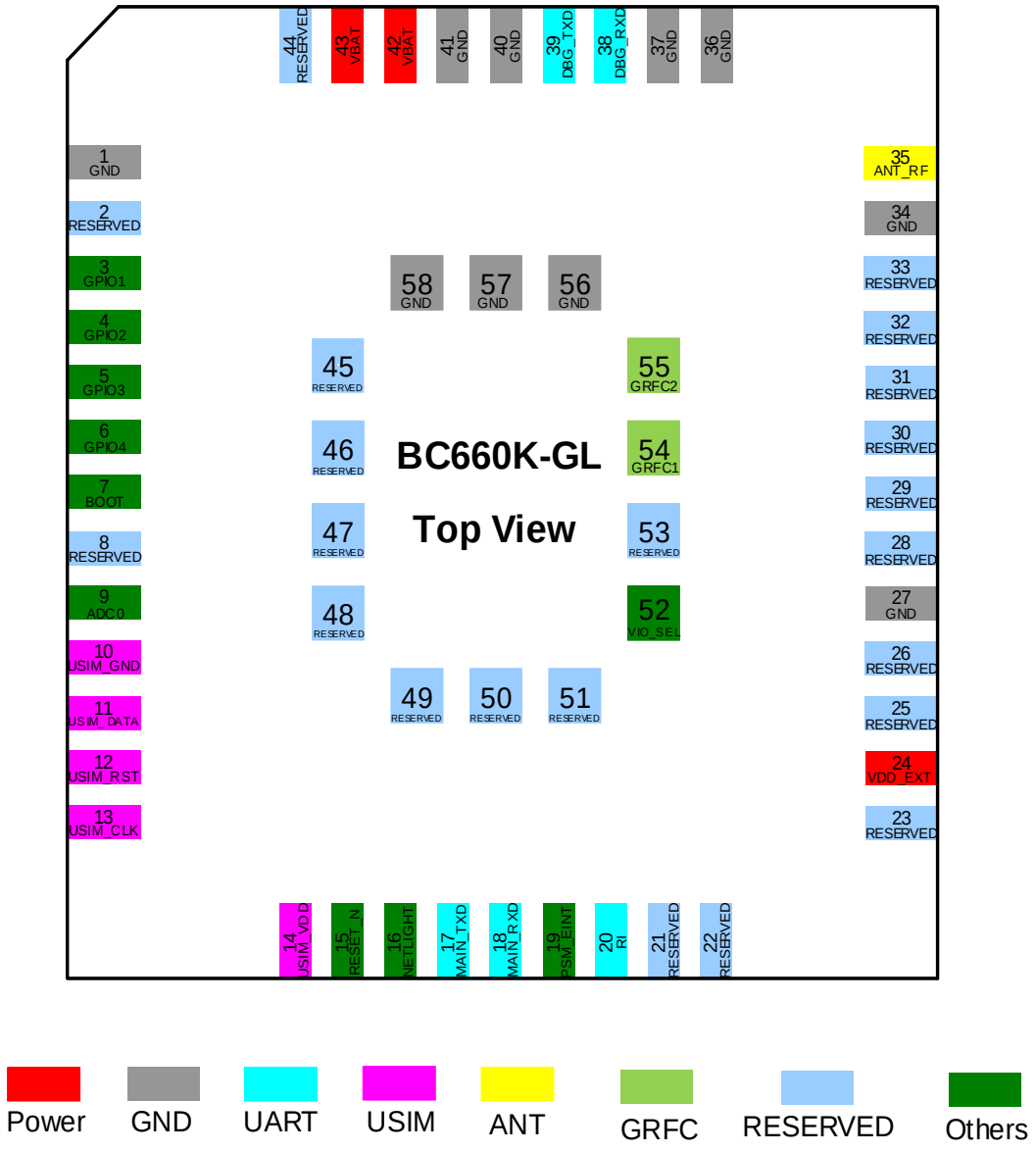


Figure 2: Pin Assignment

NOTE

Keep all RESERVED and unused pins unconnected.

3.2. Pin Description

Table 3: I/O Parameter Definition

Type	Description
AI	Analog Input
AIO	Analog Input/Output
DI	Digital Input
DO	Digital Output
DIO	Digital Input/Output
PI	Power Input
PO	Power Output

DC characteristics include power domain and rate current, etc.

Table 4: Pin Description

Power Supply					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VBAT	42, 43	PI	Power supply for the module	Vmax = 4.3 V Vmin = 2.2 V Vnom = 3.3 V	-
VDD_EXT	24	PO	1.8 V/3.1–3.3 V output power supply (Controlled by VIO_SEL, 1.8 V by default)	Vnom = 1.8 V/3.1–3.3 V Iomax = 40 mA	No voltage output in Deep/Light Sleep mode. It is intended to supply power for the module's pull-up circuits, and is not recommended to supply power for external circuits.
GND	1, 27, 34, 36, 37, 40, 41, 56–58				
BOOT					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
BOOT	7	DI	Make the module enter download mode	V_{IL}max = 0.2 × VDD_EXT V_{IH}min = 0.7 × VDD_EXT	Active low.
Reset					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESET_N	15	DI	Reset the module	V_{IL}max = 0.42 V V_{IH}min = 1.33 V V_{IH}max = 2.1 V	Active low.
PSM_EINT Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
PSM_EINT	19	DI	External interrupt pin dedicated to waking up the module from Deep/Light Sleep mode.	V_{IL}max = 0.42 V V_{IH}min = 1.33 V V_{IH}max = 2.1 V	Active on falling edge.
Network Status Indication					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
NETLIGHT	16	DO	Indicate the module's network activity status	V_{OL}max = 0.15 × VDD_EXT V_{OH}min = 0.8 × VDD_EXT	
ADC Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ADC0	9	AI	General-purpose ADC interface	Voltage range: 0–1.2 V	
Main UART					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
MAIN_RXD	18	DI	Main UART receive	V_{IL}max = 0.2 × VDD_EXT V_{IH}min = 0.7 × VDD_EXT	
MAIN_TXD	17	DO	Main UART transmit	V_{OL}max = 0.15 × VDD_EXT V_{OH}min = 0.8 × VDD_EXT	
Debug UART					

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
DBG_RXD	38	DI	Debug UART receive	V_{IL}max = 0.2 × VDD_EXT V_{IH}min = 0.7 × VDD_EXT	
DBG_TXD	39	DO	Debug UART transmit	V_{OL}max = 0.15 × VDD_EXT V_{OH}min = 0.8 × VDD_EXT	
RI					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RI	20	DO	Ring indication	V_{OL}max = 0.15 × VDD_EXT V_{OH}min = 0.8 × VDD_EXT	
USIM Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
USIM_VDD	14	PO	USIM card power supply	Vnom = 1.8/3.0 V	
USIM_CLK	13	DO	USIM card clock	V_{OL}max = 0.15 × USIM_VDD V_{OH}min = 0.8 × USIM_VDD	
USIM_RST	12	DO	USIM card reset	V_{OL}max = 0.15 × USIM_VDD V_{OH}min = 0.8 × USIM_VDD	
USIM_DATA	11	DIO	USIM card data	V_{IL}max = 0.2 × USIM_VDD V_{IH}min = 0.7 × USIM_VDD V_{OL}max = 0.15 × USIM_VDD V_{OH}min = 0.8 × USIM_VDD	
USIM_GND	10		Dedicated ground for USIM card		
Antenna Interface					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
ANT_RF	35	AIO	RF antenna interface		50 Ω characteristic impedance
GPIO Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GPIO1	3	DIO	General-purpose input/output	V_{IL}max = 0.2 × VDD_EXT V_{IH}min = 0.7 × VDD_EXT	If unused, keep these pins open.

GPIO2	4	DIO	General-purpose input/output	V_{OL}max = 0.15 × VDD_EXT V_{OH}min = 0.8 × VDD_EXT	
GPIO3	5	DIO	General-purpose input/output		
GPIO4	6	DIO	General-purpose input/output		
GRFC Interfaces					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
GRFC1	54	DO	Generic RF controller	V_{OL}max = 0.27 V V_{OH}min = 1.44 V	1.8 V power domain. If unused, keep these pins open.
GRFC2	55	DO	Generic RF controller	V_{OL}max = 0.27 V V_{OH}min = 1.44 V	
Others					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
VIO_SEL	52	DI	IO voltage selection		Control VDD_EXT voltage selection [4]
Reserved Pins					
Pin Name	**Pin No.**	**I/O**	**Description**	**DC Characteristics**	**Comment**
RESERVED	2, 8, 21–23, 25, 26, 28–33, 44–51, 53				Keep these pins open.

NOTE

1. Keep all reserved and unused pins unconnected.
2. When VIO_SEL is grounded and VBAT ≥ 3.3 V, VDD_EXT does not output the exact typical voltage of 3.3 V, the actual output voltage is between 3.1–3.3 V.

4 When VIO_SEL is grounded and VBAT < 3.3 V, VDD_EXT = VBAT;
When VIO_SEL is grounded and VBAT ≥ 3.3 V, VDD_EXT = 3.1–3.3 V;
When VIO_SEL is floating, VDD_EXT = 1.8 V.

3.3. Operating Modes

The following table briefly describes the three working modes of the module.

Table 5: Application Processor (AP) Operating Modes

Mode	Description
Normal	In normal mode, the AP handles tasks such as AT command communication.
Idle	When all tasks are suspended, the AP enters idle mode.

Table 6: Modem Operating Modes

Mode	Description
Connected	The network is connected and the module supports data transmission. In such a case, the modem can switch to DRX/eDRX mode.
DRX/eDRX	The modem is in idle mode, and downlink data can be received during PTW only. In such a case, the modem can switch to PSM or connected mode.
PSM	In power saving mode, the modem is disconnected from the network and cannot receive any downlink data. In such a case, the modem can switch to eDRX/DRX mode, then quickly switch to connected mode.

Table 7: Module Operating Modes

Mode	Description
Active	When the AP is in normal mode and the modem is in connected mode, the module is active and supports all services and functions. The current consumption in active mode is higher than that in sleep modes.
Light Sleep	Generally, when the AP is in idle mode and the modem is not in PSM mode, the module enters Light Sleep mode. In Light Sleep mode, the current consumption of the module is reduced greatly.
Deep Sleep	When the AP is in idle mode and the modem is in PSM, the module enters Deep Sleep mode in which the CPU is powered off and only the 32 kHz RTC clock keeps working. In Deep Sleep mode, the current consumption is minimized (typical value: 800 nA).

3.4. Power Saving Modes

3.4.1. Light Sleep Mode

In Light Sleep mode, the UART serial interface does not work, and the module can be woken up on the falling edge of PSM_EINT or by your sending the command **AT** to it via the main UART.

3.4.2. Deep Sleep Mode

The module consumes extremely low current in Deep Sleep mode (typical value: 800 nA). The main purpose of Deep Sleep is to reduce the power consumption of the module and prolong the power supply duration of the battery. In this mode, the UART do not work.

The following figure shows the power consumption of the module in different modes.

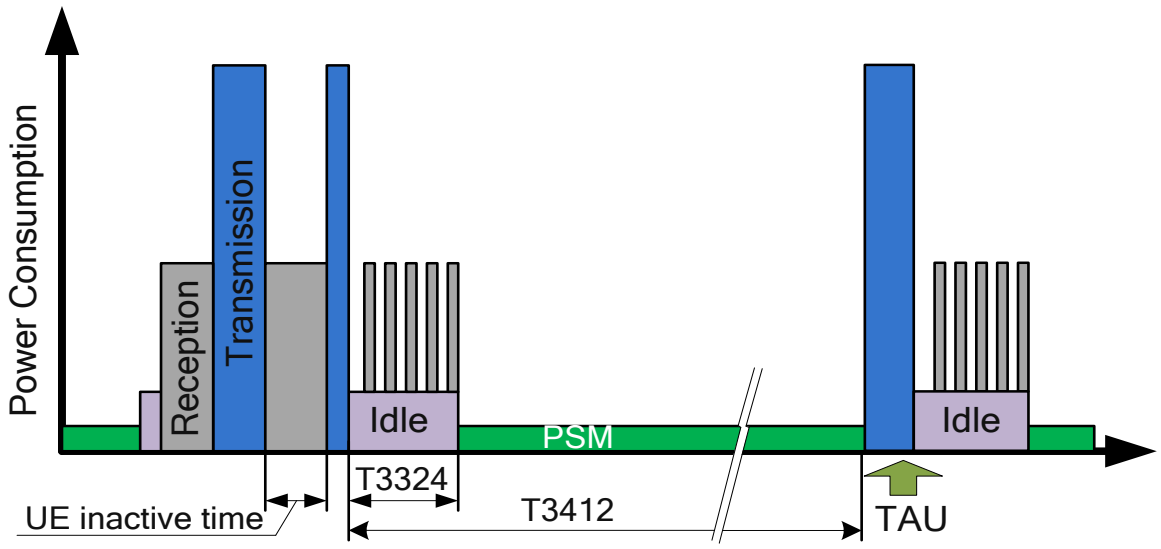


Figure 3: Module Power Consumption in Different Modem Modes

When the modem remains in PSM and the AP is in idle mode, the module will enter Deep Sleep mode.

The procedure of the modem entering PSM is as follows:

The modem requests to enable PSM with an **ATTACH REQUEST** or **TAU REQUEST** message during ATTACH or TAU (Tracking Area Update) procedure. Then the network accepts the request and provides an active time value (T3324) to the modem and the mobile reachable timer starts. When the T3324 timer expires, the modem enters PSM. Please note that the module cannot request entering PSM when establishing an emergency attachment or initializing the PDN (Public Data Network) connection.

When the module is in Deep Sleep mode, it can be woken up in the following cases:

- After the T3412 timer expires, the module will exit from Deep Sleep automatically.
- After the MCU sends an AT command to the module (this AT command will be lost), and pulls down the MAIN_RXD, the module will be woken up from Deep Sleep in MAIN_RXD's falling edge.
- Pulling down PSM_EINT (falling edge) will wake up the module from Deep Sleep.

The timing of waking up the module from Deep Sleep is illustrated below.

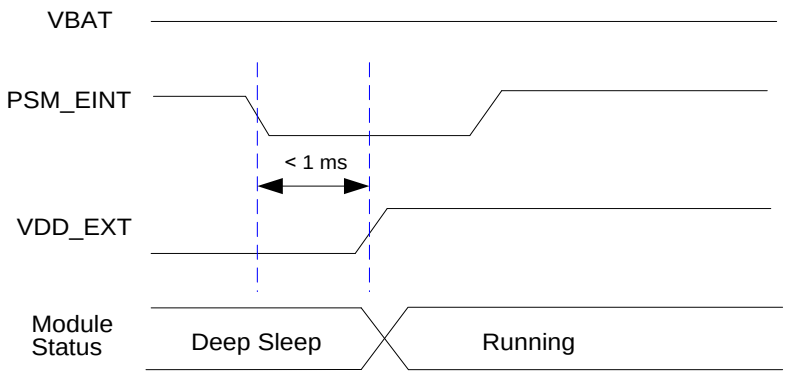


Figure 4: Timing of Waking Up Module from Deep Sleep

3.5. Power Supply

3.5.1. Power Supply Pins

The module provides two VBAT pins for connection with an external power supply. The table below describes the module's VBAT and ground pins.

Table 8: Power Supply Pins

Pin Name	Pin No.	Description	Min.	Typ.	Max.	Unit
VBAT	42, 43	Power supply for the module	2.2	3.3	4.3	V
GND	1, 27, 34, 36, 37, 40, 41, 56, 57, 58					

3.5.2. Voltage Stability Requirements

The power supply range of the module is from 2.2 V to 4.3 V. Make sure that the input voltage will never drop below 2.2 V. The following figure shows the voltage drop during heavy load.

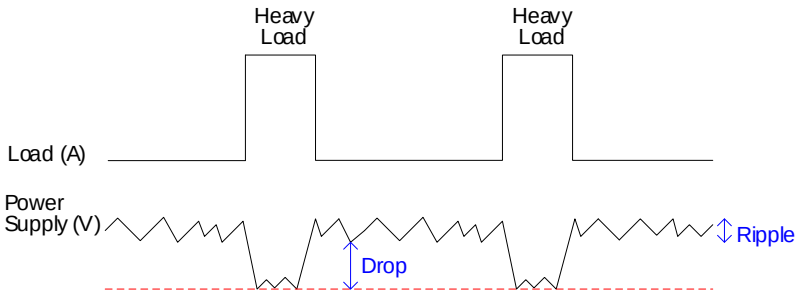


Figure 5: Power Supply Limits during Heavy Load

3.5.3. Power Supply Reference Design

Power design for a module is critical to its performance. It is recommended to use a low quiescent current LDO with an output capacity of 0.5 A to regulate the power supply for BC660K-GL. Lithium-thionyl chloride (Li-SOCl2) batteries and Lithium manganese oxide (LiMn2O4) batteries can be used as the power supply. The supply voltage of the module ranges from 2.2 V to 4.3 V. When the module is working, ensure its input voltage never drops below 2.2 V; otherwise, the module cannot work normally.

For better power performance, it is recommended to place a 100 μF tantalum capacitor with low ESR (ESR = 0.7 Ω) and three ceramic capacitors (100 nF, 100 pF and 22 pF) near the VBAT pins. Also, it is recommended to add a TVS on the VBAT trace (near VBAT pins) to improve surge voltage withstanding capability. In principle, the longer the VBAT trace is, the wider it should be. A reference circuit for power supply is illustrated in the following figure.

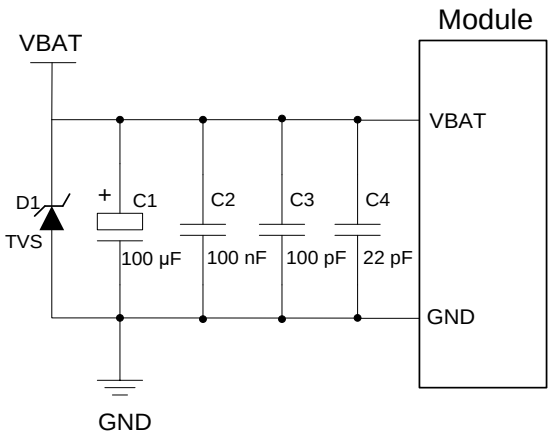


Figure 6: Reference Design for Power Supply

Table 9: TVS Selection Parameter Requirements

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Condition
V_{RWM}	Reverse operating voltage	-	-	4.85	V	-
V_{BR}	Breakdown voltage	4.9	5.3	6	V	I_{BR} = 1 mA
V_C	Clamping voltage	-	5.5	-	V	I_{PP} = 16 A (t_P = 100 ns)
V_C	Clamping voltage	-	5.5	-	V	I_{PP} = 10 A (8 × 20 μs pulse)
V_C	Clamping voltage	-	9.5	-	V	I_{PP} = 180 A (8 × 20 μs pulse)
V_C	Clamping voltage	-	7.5	-	V	V_{ESD} = 8 kV
I_R	Reverse leakage current	-	-	1.0	μA	V_{RWM} = 4.85 V

3.5.4. Power Supply Voltage Monitoring

You can use **AT+CBC** to monitor and query the current VBAT voltage. The unit of the voltage value is mV (millivolt). For detailed information about the command, see ***document [2]***.

3.6. Turn-on/Turn-off Scenario

3.6.1. Turn On

After the module VBAT is powered on, keep the RESET_N and BOOT high (both pins are at high level by default), and the module will turn on automatically. The turn-on timing is illustrated in the following figure.

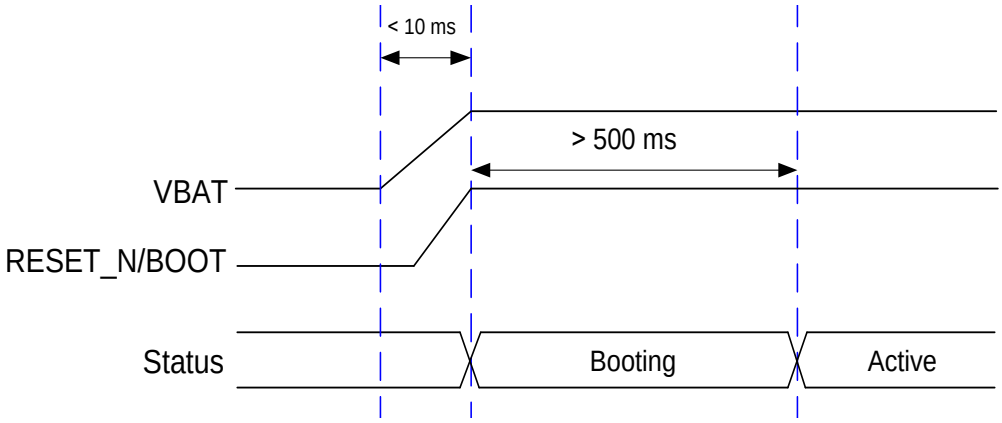


Figure 7: Turn-on Timing

NOTE

1. After the module is powered off, it can be turned on again only after its VBAT voltage drops below 0.7 V. The actual discharging time of VBAT needs to be determined based on circuit tests and enough time margin should be left to avoid abnormal module startup.
2. The power-up time of VBAT must be within 10 ms, and after VBAT is powered up, RESET_N and BOOT automatically rise to high level due to internal pull-ups.
3. It is recommended that the MCU retains a RESET_N controlling pin so that the RESET_N can reset the module to exit the abnormal state when the module is operating abnormally due to the abnormal power-up sequence or dropping supply voltage of VBAT.

3.6.2. Turn Off

The module can be turned off through cutting off its VBAT power supply.

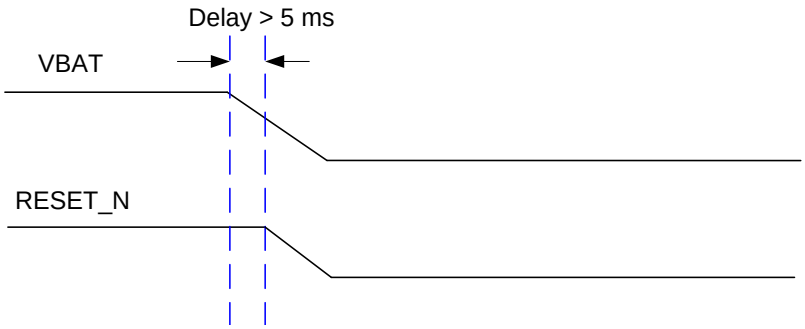


Figure 8: Turn-off Timing

3.6.3. RESET_N

Driving RESET_N low for at least 50 ms will reset the module.

Table 10: RESET_N Pin Definition

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
RESET_N	15	DI	Reset the module.	V_{IL}max = 0.42 V V_{IH}min = 1.33 V V_{IH}max = 2.1 V	Reset pull-down time ≥ 50 ms Active low.

The reference designs for resetting the module are shown below. An open drain/collector driving circuit or a button can be used to control the RESET_N pin.

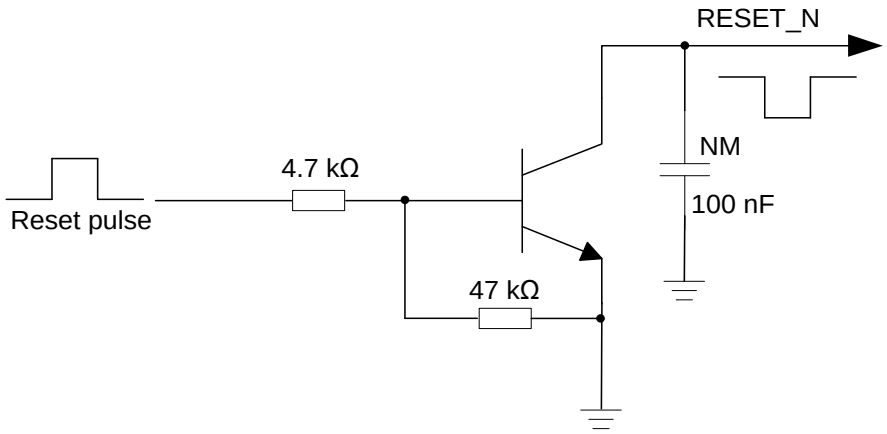


Figure 9: Reference Design for RESET_N Controlled with an OC/OD Driving Circuit

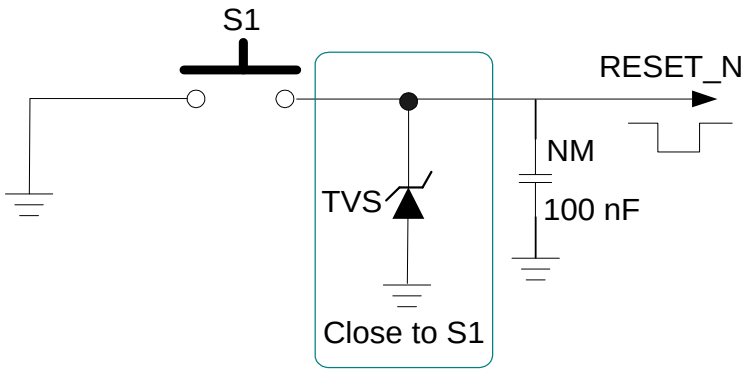


Figure 10: Reference Design for RESET_N Controlled with a Button

NOTE

It is recommended to reserve a 100 nF capacitor position; the capacitor is not mounted by default.

3.6.4. Download Mode

Table 11: BOOT Pin Definition

Pin Name	Pin No.	I/O	Description	DC Characteristics	Comment
BOOT	7	DI	Make the module enter download mode	V_{IL}max = 0.2 × VDD_EXT V_{IH}min = 0.7 × VDD_EXT	Active low.

In the process of resetting or powering on the module, drive and keep the BOOT pin low and the module

will enter the download mode.

In the download mode, the firmware can be downloaded through the main UART. After the download is completed, the module needs to be reset to exit from the download mode.

A reference design is shown below.

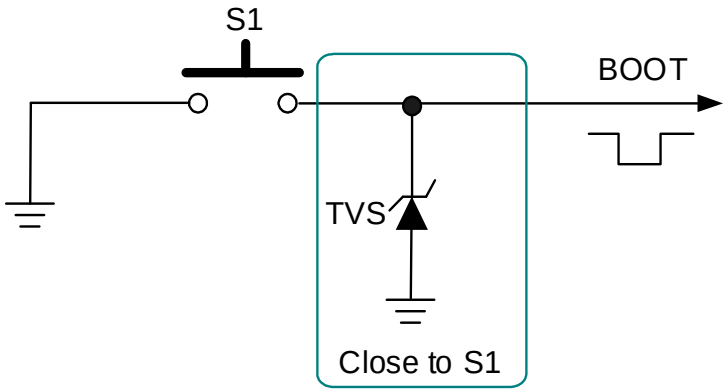


Figure 11: Reference Design for BOOT Controlled with a Button

NOTE

If the BOOT is connected to a filter capacitor in parallel, the capacitance of the capacitor cannot be higher than 33 pF.

3.7. UART

The module provides two UART: the main UART and the debug UART.

Table 12: Pin Definition of UART

Interface	Pin Name	Pin No.	I/O	Description
Main UART	MAIN_TXD	17	DO	Main UART transmit
	MAIN_RXD	18	DI	Main UART receive
Debug UART	DBG_RXD	38	DI	Debug UART receive
	DBG_TXD	39	DO	Debug UART transmit

Ring Indication	RI	20	DO	Ring indication

3.7.1. Main UART

The main UART supports AT command communication, data transmission and firmware upgrade.

- Default baud rate: 115200 bps
- Supported baud rates: 2400 bps, 4800 bps, 9600 bps, 19200 bps, 38400 bps, 57600 bps, 115200 bps, 230400 bps, 460800 bps

When the interface is used for firmware upgrade, the baud rate is 921600 bps by default.

When the module is in Deep Sleep/Light Sleep mode, the MCU can wake up it by sending AT commands through the main UART and meanwhile the MCU pulls down the MAIN_RXD. The module will be woken up from Deep Sleep in MAIN_RXD's falling edge. It is recommended to keep sending the command **AT** until **OK** is returned before sending AT commands for other services.

The figure below shows the connection between the module and the peripheral.

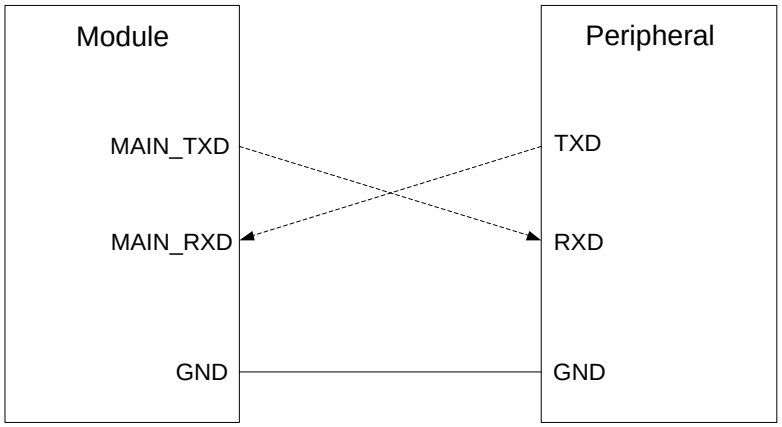


Figure 12: Reference Design for Main UART Connection

3.7.2. Debug UART

Through debug tools, the debug UART can be used to output logs for software debugging. Its baud rate is 6 Mbps by default. The following is a reference design of debug UART. This UART only supports outputting log, and cannot be used for data transmission.

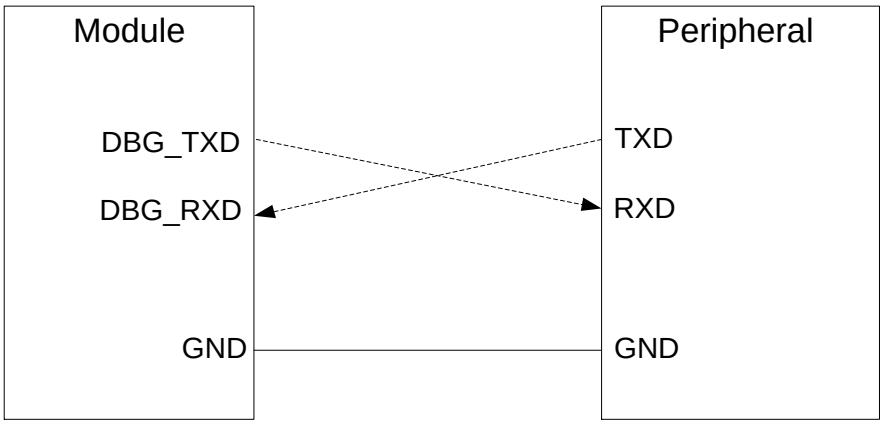


Figure 13: Reference Design for Debug UART Connection

3.7.3. UART Application

Table 13: VIO_SEL Pin Definition

Pin Name	Pin No.	I/O	Description	Comment
VIO_SEL	52	DI	IO Voltage selection	Control VDD_EXT voltage selection

The UART voltage domain of this module is optional. You can select the appropriate voltage domain through VIO_SEL according to actual situation. When VIO_SEL is floating, the VDD_EXT voltage domain is 1.8 V; when VIO_SEL is grounded, the VDD_EXT voltage domain is 3.1–3.3 V or equals to the VBAT voltage [5]. If the voltage domain of your application system is 1.8 V, VIO_SEL should be floating; If the voltage domain of your application system is 3.1–3.3 V, VIO_SEL must be grounded.

The following figure shows the reference design of UART:

5 When VIO_SEL is grounded and VBAT < 3.3 V, VDD_EXT = VBAT;
When VIO_SEL is grounded and VBAT ≥ 3.3 V, VDD_EXT = 3.1–3.3 V;
When VIO_SEL is floating, VDD_EXT = 1.8 V.

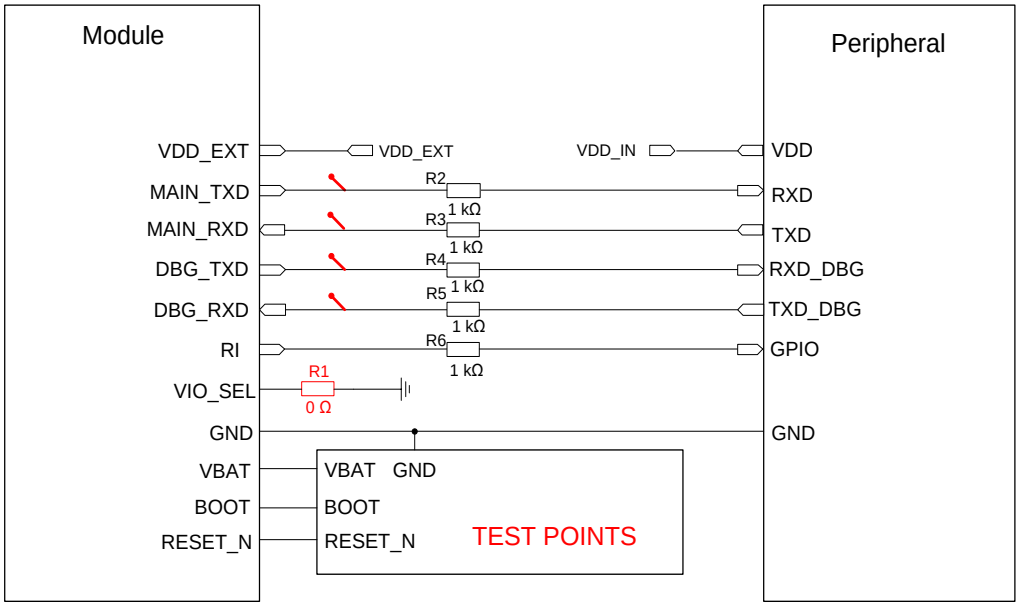


Figure 14: Reference Design for UART Connection

The following circuit shows a reference design for the communication between the module and a PC with a standard RS-232 interface. Make sure to select appropriate voltage domain through VIO_SEL according to the actual situation.

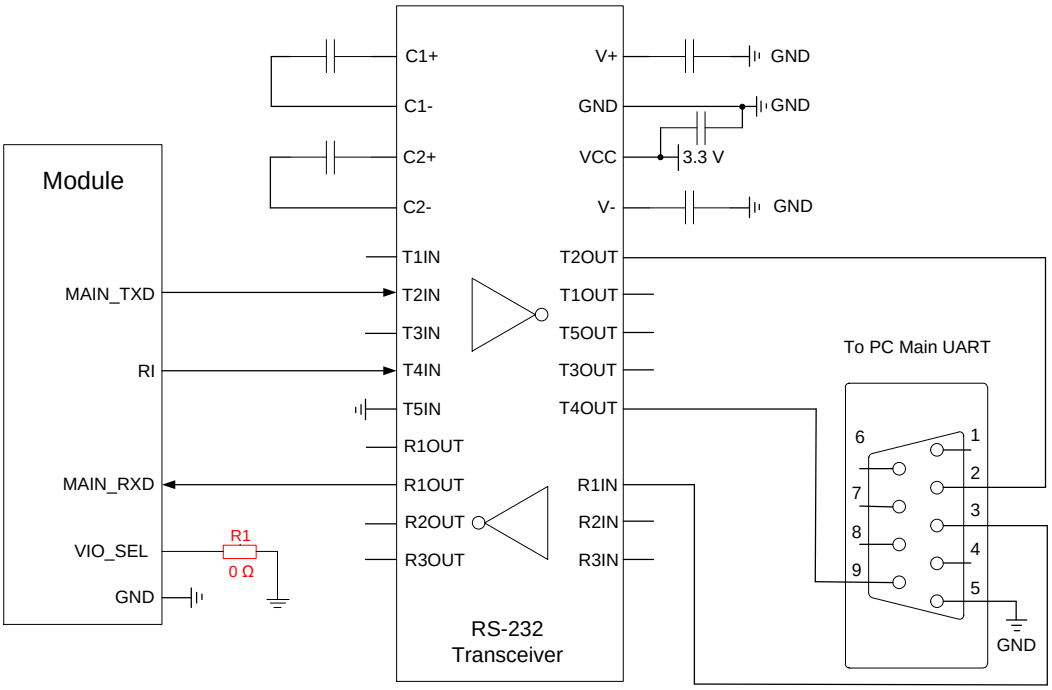


Figure 15: Reference Design for Module-PC Communication via RS-232 Interface

Please visit vendors' websites to select a suitable RS-232 transceiver, such as http://www.exar.com and

http://www.maximintegrated.com.

NOTE

1. If the voltage domain of your application system is 1.8 V, keep the R1 in red not mounted; if it is 3.1-3.3 V, keep the R1 in red mounted.
2. "\" represents the test points of UART. It is recommended to reserve the test points of VBAT, BOOT and RESET_N for convenient firmware upgrade and software debugging when necessary.
3. MAIN_RXD cannot be pulled up to VDD_EXT directly. To pull up MAIN_RXD to VDD_EXT, you need to connect a Schottky diode in series first, and then add a pull-up resistor of 4.7–20 kΩ. For more details, see ***document [3]***.

If the voltage domain of your application system is neither 1.8 V nor 3.1–3.3 V, it is recommended to use a level-shifting circuit. For the design of the circuit shown in the dotted line, refer to that shown in the solid lines, and pay attention to the connection direction. In this case, the design of RI–GPIO circuit can refer to that of the MAIN_TXD–RXD circuit.

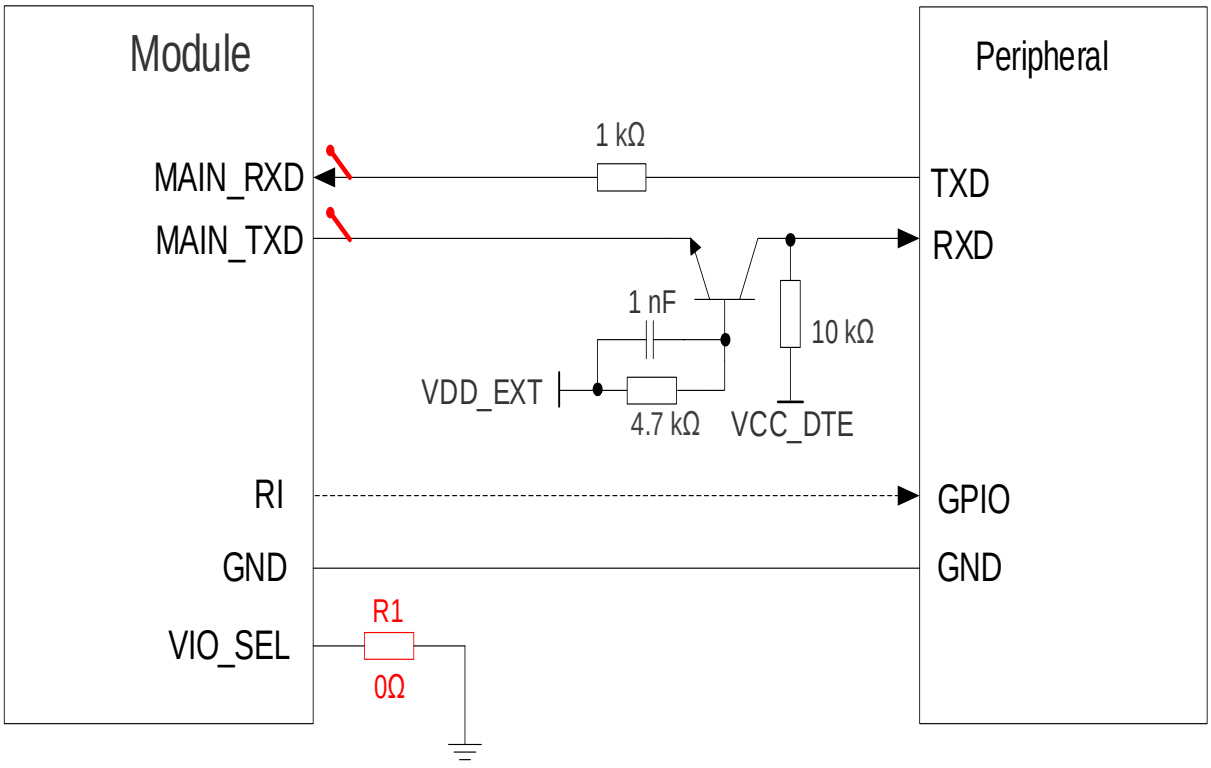


Figure 16: Reference Design for Level-shifting Circuit

NOTE

1. Due to the anti-backflow design of the MAIN_RXD pin, it can be directly connected to the TXD of the peripheral in 1.8–3.3 V voltage domain. If wake-up function of MAIN_RXD in Deep Sleep/Light Sleep mode is enabled, it is recommended that MAIN_RXD not use any level-shifting circuit so as to avoid abnormal wake-up.
2. If you apply the level-shifting circuit, don't mount the R1 marked in red.
3. MAIN_RXD cannot be pulled up to VDD_EXT directly. To pull up MAIN_RXD to VDD_EXT, you need to connect a Schottky diode in series first, and then add a pull-up resistor of 4.7–20 kΩ. For more details, see ***document [3]***.
4. The level-shifting circuit does not apply to applications with high baud rates exceeding 460 kbps.

3.8. USIM Interface

The USIM card is powered by USIM_VDD. Both 1.8 V and 3.0 V USIM cards are supported.

Table 14: Pin Definition of USIM Interface

Pin Name	Pin No.	I/O	Description	Comment
USIM_VDD	14	PO	USIM card power supply	When 3.0 V ≤ VBAT ≤ 4.3 V, supports 1.8/3.0 V USIM card; When 2.2 V ≤ VBAT < 3 V, only supports 1.8 V USIM card; Maximum supply current: about 80 mA.
USIM_CLK	13	DO	USIM card clock	
USIM_RST	12	DO	USIM card reset	
USIM_DATA	11	DIO	USIM card data	
USIM_GND	10		Dedicated ground for USIM card	

A reference design for the USIM interface with a 6-pin USIM card connector is below.

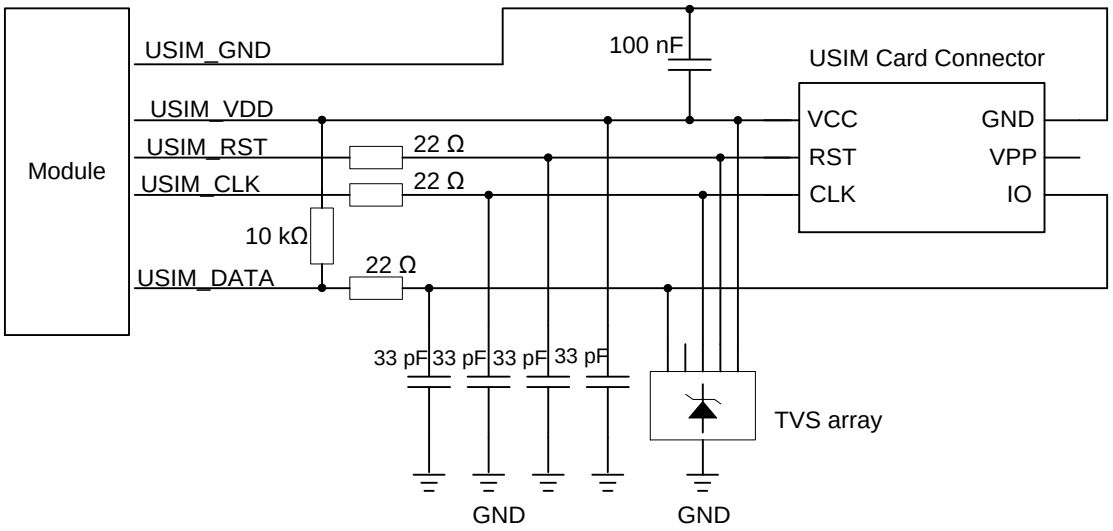


Figure 17: Reference Design for USIM Interface with a 6-pin USIM Card Connector

To enhance the reliability and availability of the USIM card in applications, follow the criteria below in USIM circuit design:

- Place the USIM card connector as close to the module as possible. Keep the trace length as short as possible, at most 200 mm.
- Keep USIM card signal lines away from RF and power supply traces.
- Make the trace between the ground of the module and that of the USIM card connector short and wide and ensure the trace width not less than 0.5 mm avoid any decrease in electric potential. The decoupling capacitor between USIM_VDD and GND should be not more than 1 μF and be placed close to the USIM card connector.
- To avoid cross-talk between USIM_DATA and USIM_CLK, keep them away from each other and shield them separately with surrounding ground.
- For better ESD protection, it is recommended to add a TVS array whose parasitic capacitance should be not more than 50 pF. Place the ESD protection component as close to the USIM card connector as possible, and ensure the USIM card signal lines from the USIM card connector go through the ESD protection component before reaching the module. The 22 Ω resistors should be connected in series between the module and the USIM card connector to suppress EMI spurious transmission and enhance ESD protection. Note that the module's USIM peripheral devices should be placed close to the USIM card connector.

NOTE

The pull-up resistor of 10 kΩ on the USIM_DATA can improve anti-jamming capability and should be placed close to the USIM card connector.

3.9. ADC Interface

The module provides a 12-bit ADC input channel to read the voltage value.

Table 15: Pin Definition of ADC Interface

Pin Name	Pin No.	I/O	Description	Comment
ADC0	9	AI	General-purpose ADC interface	Voltage range: 0–1.2 V.

NOTE

A 320 kΩ pull-down resistor is integrated inside the ADC0 pin. This resistor needs to be considered when you calculate the voltage division relationship.

3.10. RI

When there is a message received or a URC output, the module will notify the peripheral through the RI interface.

Table 16: Pin Definition of RI Interface

Pin Name	Pin No.	I/O	Description	Comment
RI	20	DO	Ring indication	VDD_EXT power domain

Table 17: RI Signal Status

Module Status	RI Signal Level
Idle	High
URC/SMS Message Arrives	Low for at least 120 ms before starting data output.

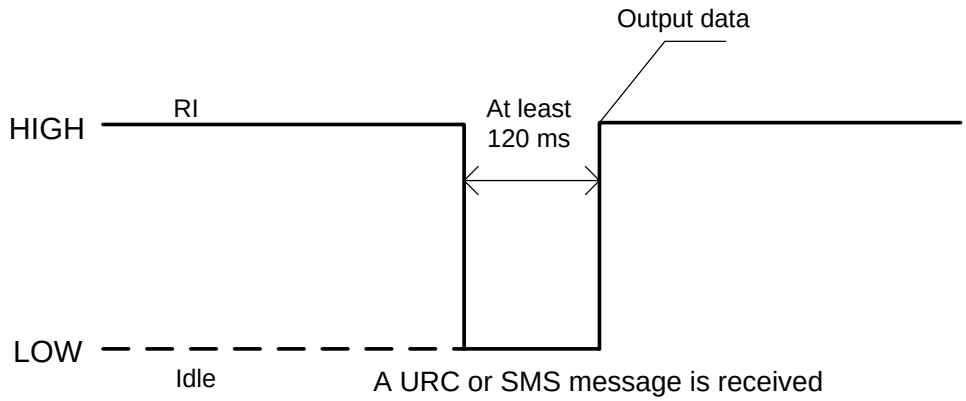


Figure 18: RI Behaviour When a URC/SMS Message Is Received

3.11. GPIO Interfaces

The module provides four general-purpose input and output (GPIO) interfaces. **AT+QCFG="gpio"** command can be used to configure the status of the GPIO pins. For more details about the AT command, see ***document [2]***.

Table 18: Pin Definition of GPIO Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GPIO1	3	DIO	General-purpose input/output	If unused, keep these pins open.
GPIO2	4	DIO		
GPIO3	5	DIO		
GPIO4	6	DIO		

3.12. GRFC Interfaces

The module provides two generic RF control interfaces for the control of external antenna tuners.

Table 19: Pin Definition of GRFC Interfaces

Pin Name	Pin No.	I/O	Description	Comment
GRFC1	54	DO	Generic RF controller	1.8 V power domain. If unused, keep these pins open.
GRFC2	55	DO	Generic RF controller	

Table 20: Truth Table of GRFC Interfaces

GRFC1 Level	GRFC2 Level	Frequency Range (MHz)	Band
Low	Low	880–2180	B1, B2, B3, B4, B8, B25, B66, B70
Low	High	791–894	B5, B18, B19, B20
High	Low	698–803	B12, B13, B17, B28, B85
High	High	-	Disabled

3.13. NETLIGHT

NETLIGHT can be used to indicate the network status of the module.

Table 21: Pin Definition of NETLIGHT

Pin Name	Pin No.	I/O	Description	Comment
NETLIGHT	16	DO	Indicate the module's network activity status	V_{OL}max = 0.15 × VDD_EXT V_{OH}min = 0.8 × VDD_EXT

A reference design for NETLIGHT is shown below.

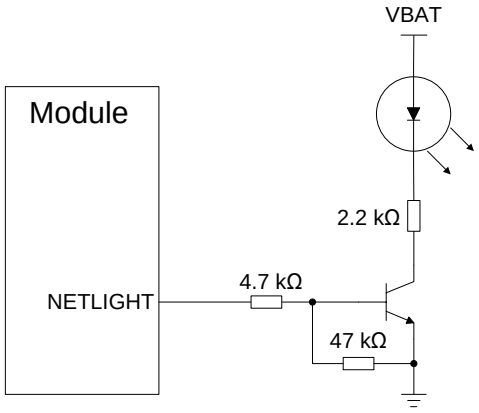


Figure 19: Reference Design for NETLIGHT

4 RF Specifications

The pin 35 is the RF antenna pad. The antenna interface has an impedance of 50 Ω.

Appropriate antenna type and design should be used with matched antenna parameters according to specific application. It is required to perform a comprehensive functional test for the RF design before mass production of terminal products. The entire content of this chapter is provided for illustration only. Analysis, evaluation and determination are still necessary when designing target products.

4.1. Antenna Interface

Table 22: Pin Definition of NB-IoT Antenna Interface

Pin Name	Pin No.	I/O	Description
ANT_RF	35	AIO	RF antenna interface
GND	34, 36, 37		Ground

4.2. Operating Frequency

Table 23: Module Operating Frequency

Frequency Band	Receiving Frequency	Transmitting Frequency
B1	2110–2170 MHz	1920–1980 MHz
B2	1930–1990 MHz	1850–1910 MHz
B3	1805–1880 MHz	1710–1785 MHz
B4	2110–2155 MHz	1710–1755 MHz
B5	869–894 MHz	824–849 MHz

B8	925–960 MHz	880–915 MHz
B12	729–746 MHz	699–716 MHz
B13	746–756 MHz	777–787 MHz
B17	734–746 MHz	704–716 MHz
B18	860–875 MHz	815–830 MHz
B19	875–890 MHz	830–845 MHz
B20	791–821 MHz	832–862 MHz
B25	1930–1995 MHz	1850–1915 MHz
B28	758–803 MHz	703–748 MHz
B66	2110–2180 MHz	1710–1780 MHz
B70	1995–2020 MHz	1695–1710 MHz
B85	728–746 MHz	698–716 MHz

4.3. Reference Design

BC660K-GL provides an RF antenna pin for external NB-IoT antenna connection.

- The RF trace on the host PCB should be a coplanar waveguide or microstrip whose characteristic impedance is 50 Ω.
- The module comes with ground pads which are next to the antenna pad to give a better grounding.
- To achieve better RF performance, it is recommended to reserve a π type matching circuit and place the π-type matching components (R1/C1/C2) as close to the antenna as possible. By default, the capacitors (C1/C2) are not mounted and a 0 Ω resistor is mounted on R1.

A reference design of the RF interface is shown below.

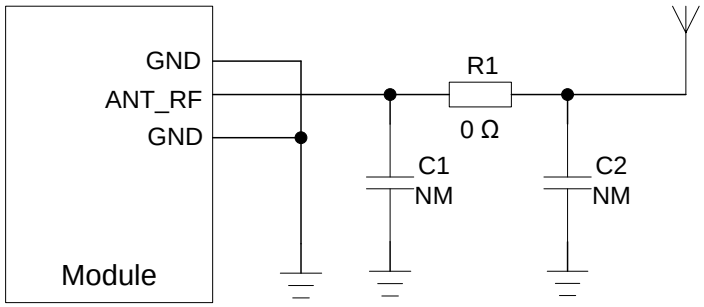


Figure 20: Reference Design for the Antenna Interface

4.4. RF Routing Guidelines

The characteristic impedance of all RF traces on your PCB should be controlled at 50 Ω. The impedance of the RF traces is usually determined by the trace width (W), the material's dielectric constant, the height from the reference ground to the signal layer (H), and the clearance between RF traces and grounds (S). The microstrip or coplanar waveguide is typically used in RF layout to control characteristic impedance. The following are reference designs for microstrip or coplanar waveguide transmission lines with different PCB structures.

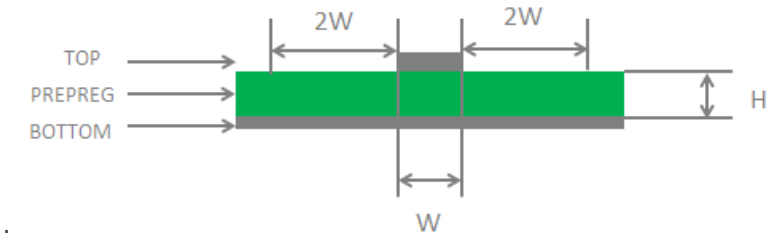


Figure 21: Microstrip on a 2-layer PCB

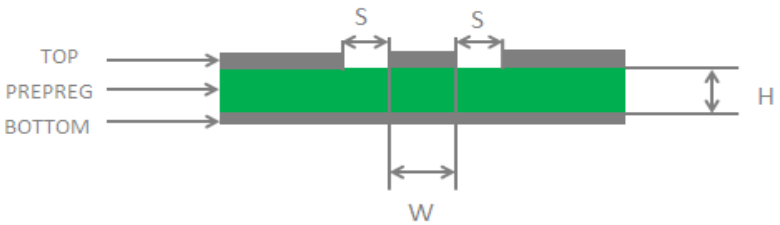


Figure 22: Coplanar Waveguide on a 2-layer PCB

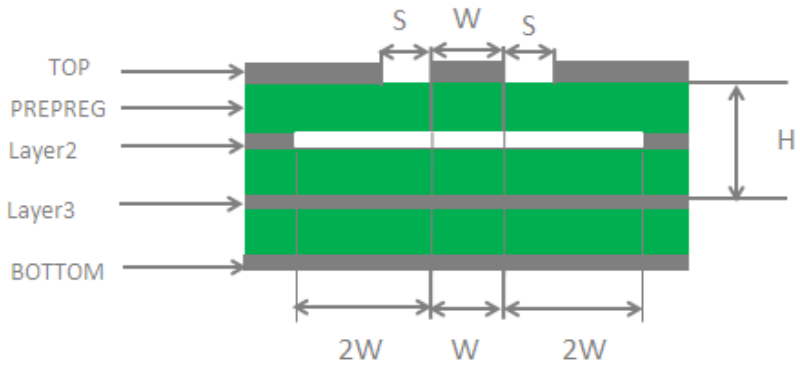


Figure 23: Coplanar Waveguide on a 4-layer PCB (Layer 3 as Reference Ground)

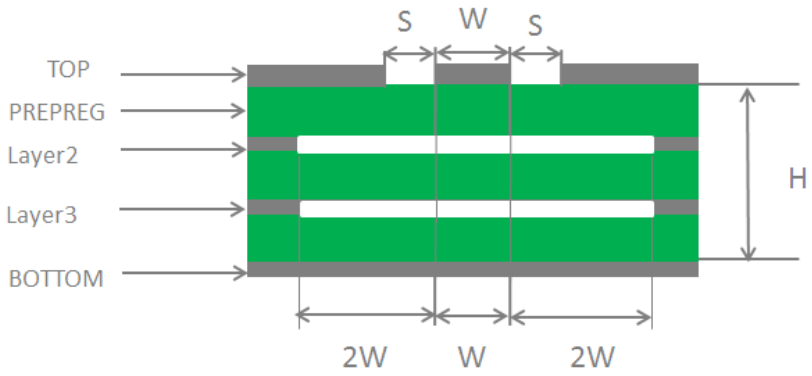


Figure 24: Coplanar Waveguide on a 4-layer PCB (Bottom Layer as Reference Ground)

To ensure reliable RF performance, the following principles should be complied with in RF layout design:

- Use an impedance simulation tool to accurately control the characteristic impedance of RF traces at 50 Ω.
- The GND pins adjacent to the RF pin should not be designed as thermal relief pads, and should be fully grounded.
- The distance between the RF pin and the RF connector should be as short as possible, and all the right-angle traces should be changed to curve ones. The recommended trace angle is 135°.
- There should be clearance under the signal pin of the antenna connector or solder joint.
- The reference ground of RF traces should be complete. Meanwhile, adding some ground vias around RF traces and the reference ground helps to improve RF performance. The distance between the ground vias and RF traces should be not less than twice as wide as RF signal traces (2 × W).
- Keep RF traces away from interference sources, and avoid intersection and paralleling between traces on adjacent layers.

For more details on the reference design of RF Layout, see ***document [4]***.

4.5. Antenna Design Requirements

To minimize the loss on RF trace and RF cable, pay attention to the antenna design. The following tables show the requirements on an NB-IoT antenna.

Table 24: Antenna Cable Insertion Loss Requirements

Band	Requirements
LTE B5/B8/B12/B13/B17/B18/B19/B20/B28/B85	Cable insertion loss: < 1 dB
LTE B1/B2/B3/B4/B25/B66/B70	Cable insertion loss: < 1.5 dB

Table 25: Required Antenna Parameters

Parameter	Requirements
Frequency Range	698–2180 MHz
VSWR	≤ 2
Efficiency	> 30 %
Max. Input Power (W)	50
Input Impedance (Ω)	50

4.6. Transmitting Power

Table 26: Transmitting Power

Frequency Band	Max.	Min.
B1/B2/B3/B4/B5/B8/B12/B13/B17/B18/ B19/B20/B25/B28/B66/B70/B85	23 dBm ±2 dB	< -39 dBm

NOTE

The design conforms to the NB-IoT radio protocols in 3GPP Rel-13 and Rel-14.

4.7. Receiver Sensitivity

Table 27: Receiver Sensitivity without Retransmission (Throughput ≥ 95 %)

Frequency Band	Receiver Sensitivity	3GPP Requirement
B1/B2/B3/B4/B5/B8/B12/B13/B17/B18/B19/ B20/B25/B28/B66/B70/B85	-116 dBm	-107.5 dBm

Table 28: Receiver Sensitivity in 128 Retransmission (Throughput ≥ 95 %)

Frequency Band	Receiving Sensitivity
B1/B2/B3/B4/B5/B8/B12/B13/B17/B18/B19/B20/B25/B28/B66/B70/B85	≤ -129 dBm

4.8. RF Connector Recommendation

If RF connector is used for antenna connection, it is recommended to use the U.FL-R-SMT connector provided by Hirose.

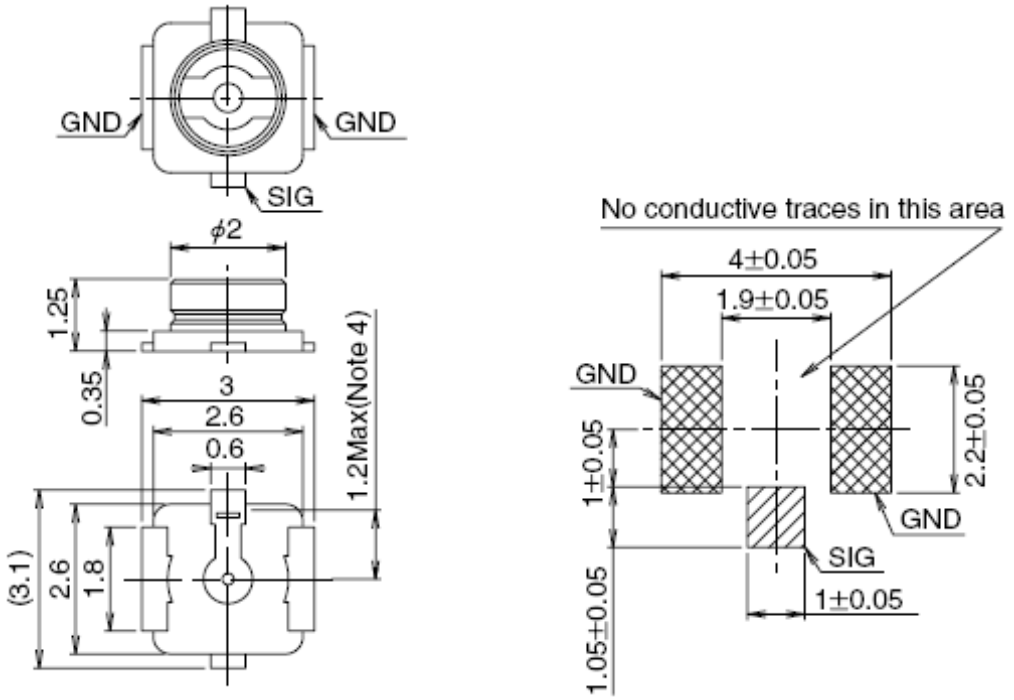


Figure 25: Dimensions of the Receptacle (Unit: mm)

U.FL-LP series mated plugs listed in the following figure can be used to match the U.FL-R-SMT.

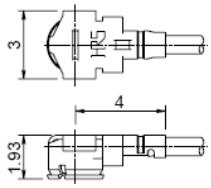
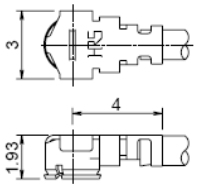
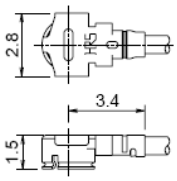
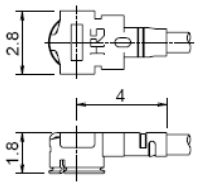
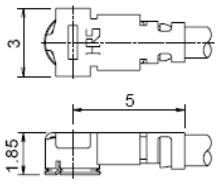
Part No.	U.FL-LP-040	U.FL-LP-066	U.FL-LP(V)-040	U.FL-LP-062	U.FL-LP-088
					
Mated Height	2.5mm Max. (2.4mm Nom.)	2.5mm Max. (2.4mm Nom.)	2.0mm Max. (1.9mm Nom.)	2.4mm Max. (2.3mm Nom.)	2.4mm Max. (2.3mm Nom.)
Applicable cable	Dia. 0.81mm Coaxial cable	Dia. 1.13mm and Dia. 1.32mm Coaxial cable	Dia. 0.81mm Coaxial cable	Dia. 1mm Coaxial cable	Dia. 1.37mm Coaxial cable
Weight (mg)	53.7	59.1	34.8	45.5	71.7
RoHS	YES				

Figure 26: Specifications of Mated Plugs

The following figure describes the space factor of mated connectors.

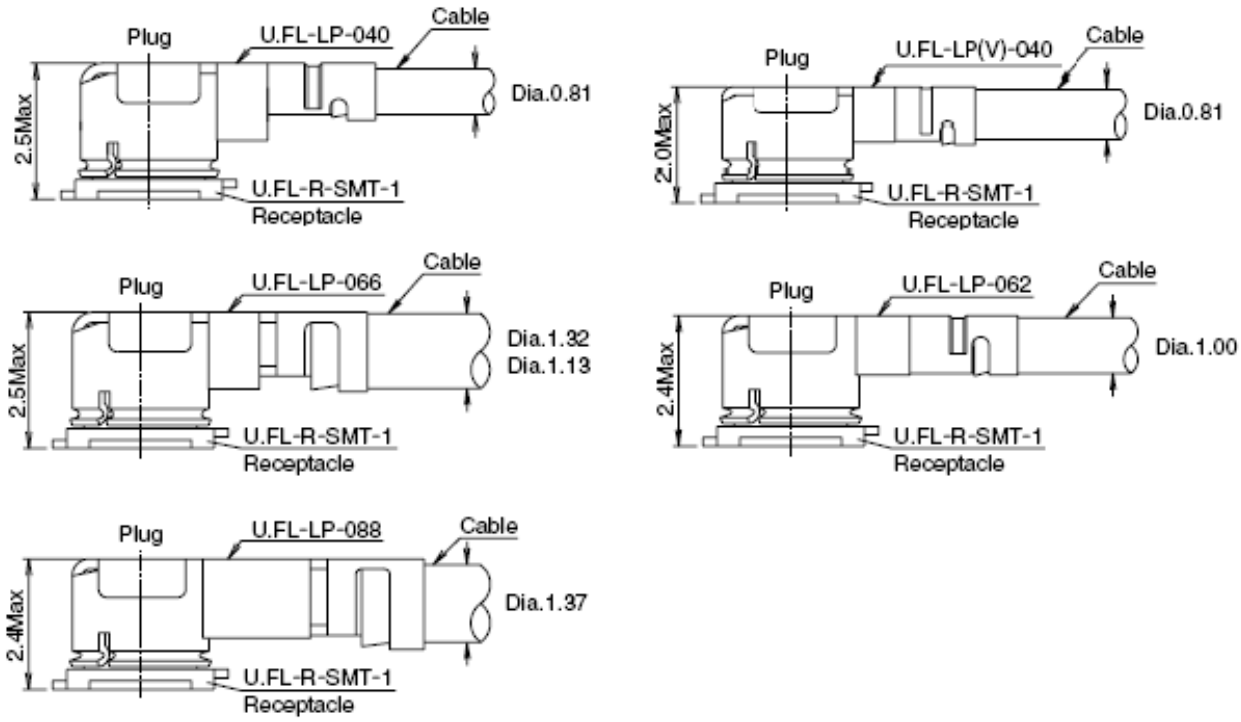


Figure 27: Space Factor of Mated Connectors (Unit: mm)

For more details, visit http://www.hirose.com.

5 Electrical Characteristics and Reliability

5.1. Absolute Maximum Ratings

Absolute maximum ratings for power supply and voltage on digital and analog pins of the module are listed in the following table.

Table 29: Absolute Maximum Ratings

Parameter	Min.	Max.	Unit
VBAT	-0.3	4.5	V
Voltage at Digital Pins	-0.3	3.6	V
Voltage at Analog Pins	-0.3	3.6	V

5.1. Operating and Storage Temperatures

The following table lists the operating and storage temperatures of the module.

Table 30: Operating and Storage Temperatures

Parameter	Min.	Typ.	Max.	Unit
Operating Temperature Range [6]	-35	+25	+75	ºC

6 Within the operating temperature range, the module meets 3GPP specifications.

Extended Temperature Range [7]	-40	-	+85	ºC
Storage Temperature Range	-40	-	+90	ºC

5.2. Power Consumption

The table below lists the power consumption of BC660K-GL under different states.

Table 31: Module Power Consumption (3.3 V VBAT Power Supply)

Deep Sleep						
AP Mode	**Modem Mode**		**Min.**	**Typ.**	**Max.**	**Unit**
Idle	PSM		-	0.8	-	μA
Light Sleep						
AP Mode	**Modem Mode**		**Min.**	**Typ.**	**Max.**	**Unit**
Idle	eDRX = 40.96 s, PTW = 10.24 s, ECL = 0		-	38	-	μA
	@ DRX = 1.28 s, ECL = 0		-	220	-	μA
	@ DRX = 2.56 s, ECL = 0		-	110	-	μA
Active [8]						
AP Mode	**Modem Mode**		**Min.**	**Typ.**	**Max. [9]**	**Unit**
Normal	Single-tone (15 kHz subcarrier spacing)	B1 @ 23.4 dBm	-	111	300	mA
		B2 @ 22.5 dBm	-	108	305	mA
		B3 @ 22.5 dBm	-	100	280	mA
		B4 @ 22.5 dBm	-	100	277	mA
		B5 @ 23.2 dBm	-	98	270	mA

7 Within the extended temperature range, the module remains the ability to establish and maintain functions such as SMS, data transmission, etc., without any unrecoverable malfunction. Radio spectrum and radio network are not influenced, while one or more specifications, such as P_{out}, may exceed the specified tolerances of 3GPP. When the temperature returns to the operating temperature range, the module meets 3GPP specifications again.

8 Power consumption under laboratory instrument test condition.

9 The “maximum value” in “Active” mode refers to the maximum pulse current during RF emission.

	B8 @ 23.1 dBm	-	105	299	mA
	B12 @ 23.3 dBm	-	120	332	mA
	B13 @ 23.2 dBm	-	100	283	mA
	B17 @ 23.2 dBm	-	115	325	mA
	B18 @ 23.2 dBm	-	94	265	mA
	B19 @ 23.2 dBm	-	95	270	mA
	B20 @ 23.2 dBm	-	98	272	mA
	B25 @ 22.5 dBm	-	108	301	mA
	B28 @ 23.3 dBm	-	109	310	mA
	B66 @ 22.5 dBm	-	101	280	mA
	B70 @ 22.6 dBm	-	104	276	mA
	B85 @ 23.2 dBm	-	115	329	mA
Single-tone (3.75 kHz subcarrier spacing)	B1 @ 23.2 dBm	-	240	311	mA
	B2 @ 22.7 dBm	-	230	296	mA
	B3 @ 22.8 dBm	-	213	274	mA
	B4 @ 23 dBm	-	212	273	mA
	B5 @ 22.9 dBm	-	202	263	mA
	B8 @ 22.8 dBm	-	221	298	mA
	B12 @ 23.1 dBm	-	259	328	mA
	B13 @ 22.8 dBm	-	218	279	mA
	B17 @ 23.1 dBm	-	252	325	mA
	B18 @ 23.1 dBm	-	199	258	mA
	B19 @ 22.9 dBm	-	201	260	mA
	B20 @ 22.9 dBm	-	207	267	mA
	B25 @ 22.7 dBm	-	232	297	mA

	B28 @ 23.1 dBm	-	240	306	mA
	B66 @ 22.8 dBm	-	213	274	mA
	B70 @ 22.7 dBm	-	216	273	mA
	B85 @ 23 dBm	-	252	323	mA

5.3. Digital I/O Characteristics

Table 31: USIM I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	0.7 × USIM_VDD	-	V
V_{IL}	Input low voltage	-	0.2 × USIM_VDD	V
V_{OH}	Output high voltage	0.8 × USIM_VDD	-	V
V_{OL}	Output low voltage	-	0.15 × USIM_VDD	V

Table 32: Other I/O Requirements

Parameter	Description	Min.	Max.	Unit
V_{IH}	Input high voltage	0.7 × VDD_EXT	-	V
V_{IL}	Input low voltage	-	0.2 × VDD_EXT	V
V_{OH}	Output high voltage	0.8 × VDD_EXT	-	V
V_{OL}	Output low voltage	-	0.15 × VDD_EXT	V

5.4. ESD Protection

Static electricity occurs naturally and it may damage the module. Therefore, applying proper ESD countermeasures and handling methods is imperative. For example, wear anti-static gloves during the development, production, assembly and testing of the module; add ESD protection components to the ESD sensitive interfaces and points in the product design.

Table 33: Electrostatic Discharge Characteristics (Temperature: 25–30 ºC, Humidity: 45 ±5 %)

Tested Interface	Contact Discharge	Air Discharge	Unit
VBAT, GND	±5	±10	kV
Antenna interface	±5	±10	kV
Other interfaces	±0.5	±1	kV

6 Mechanical Information

This chapter describes the mechanical dimensions of the module. All dimensions are measured in millimeter (mm), and the dimensional tolerances are ±0.2 mm unless otherwise specified.

6.1. Mechanical Dimensions

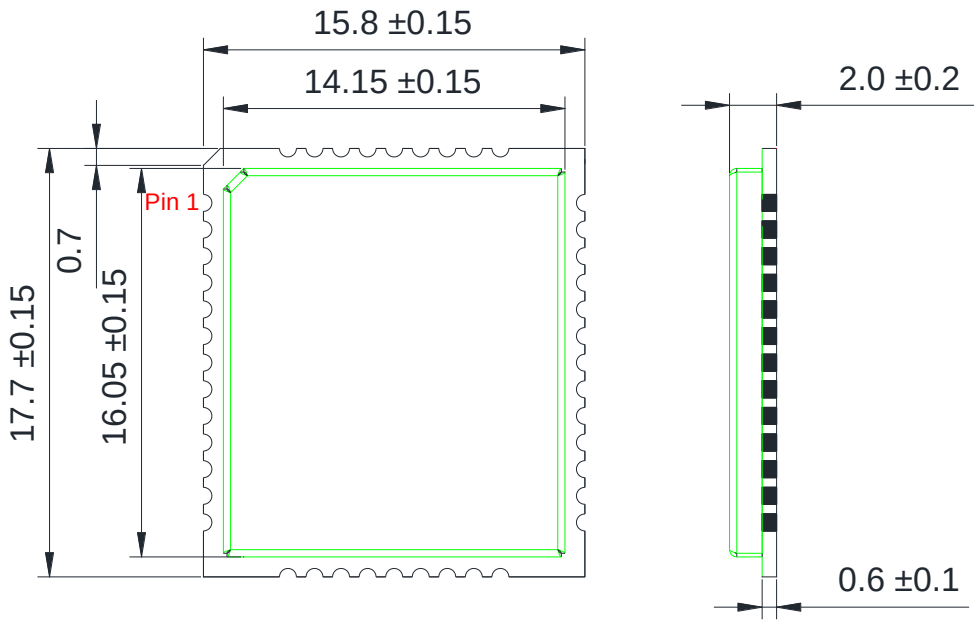


Figure 28: Module Top and Side Dimensions

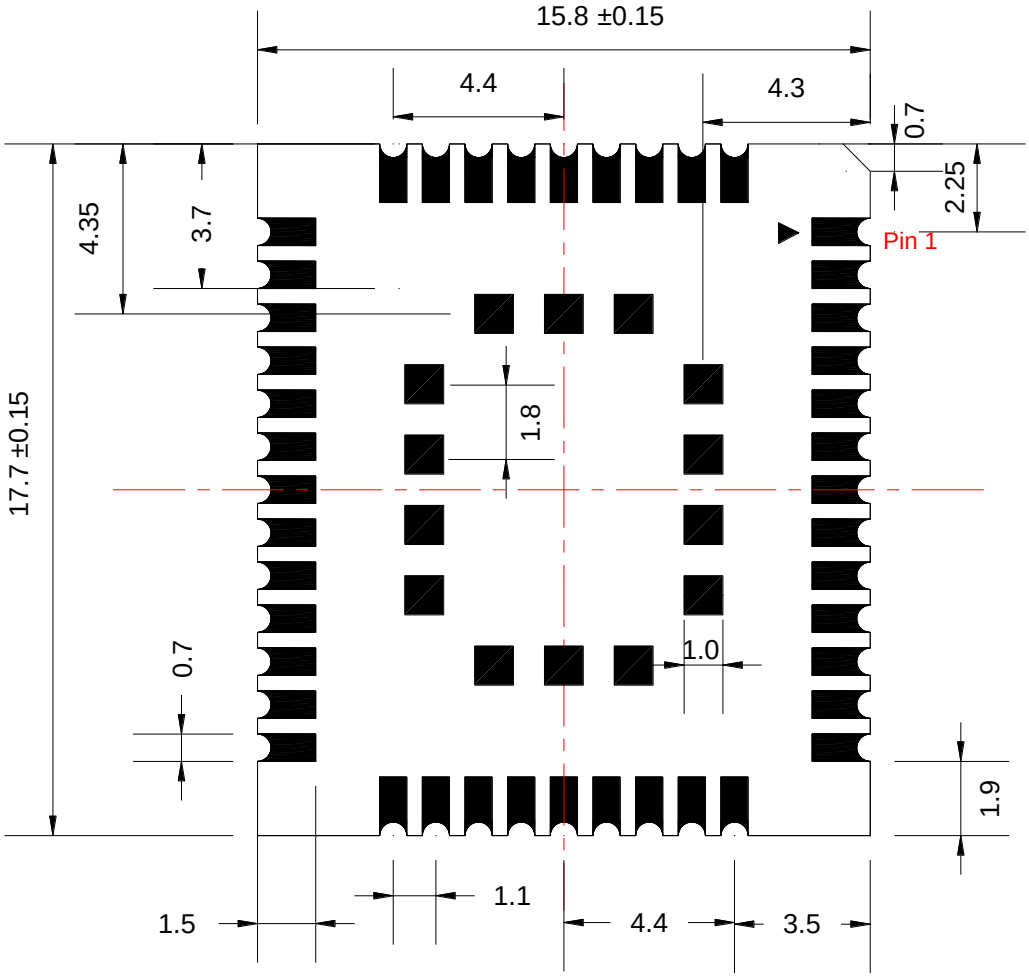


Figure 29: Module Bottom Dimensions (Bottom View)

NOTE

The package warpage level of the module conforms to *JEITA ED-7306* standard.

6.2. Recommended Footprint

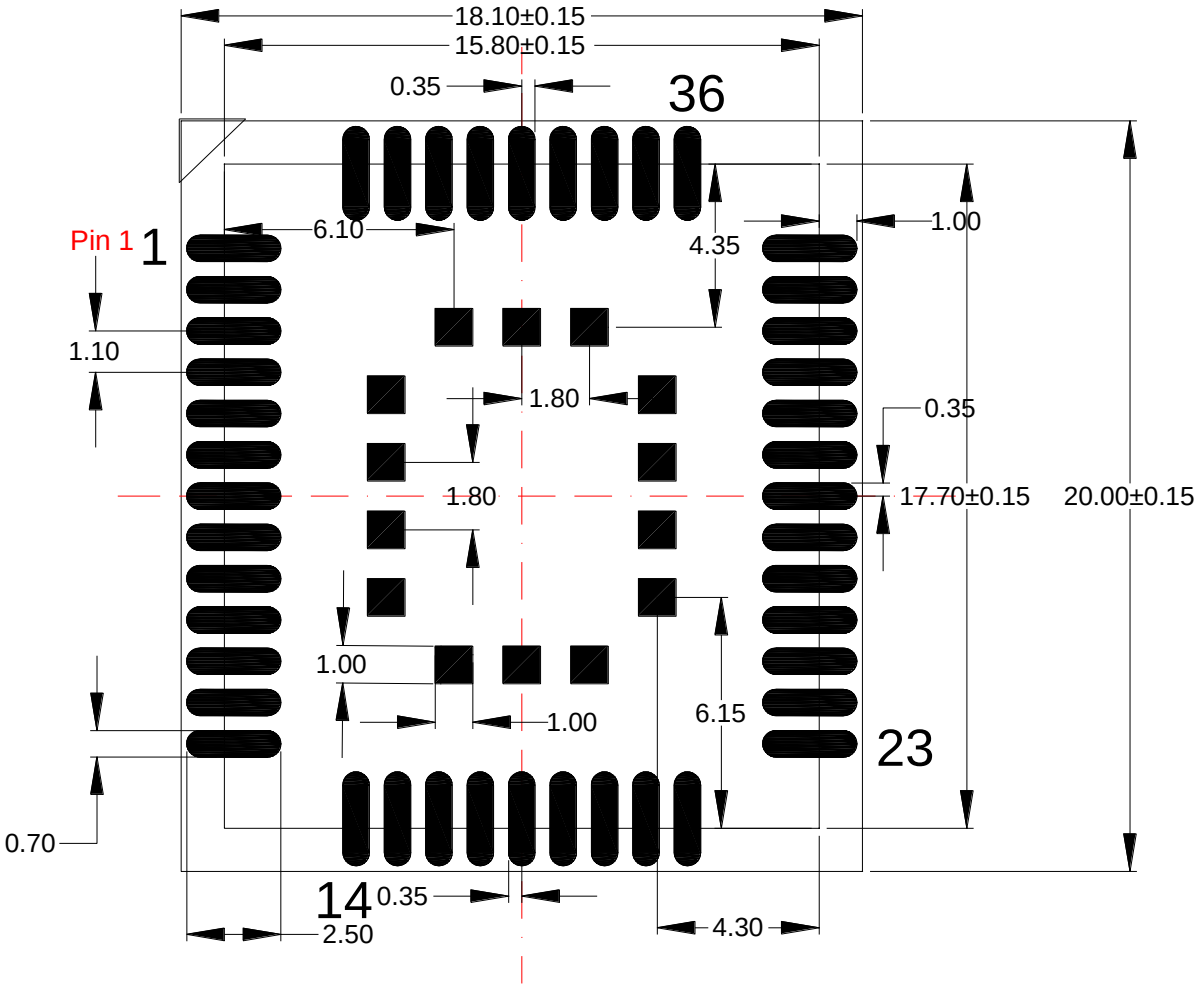


Figure 30: Recommended Footprint

NOTE

Keep at least 3 mm between the module and other components on the motherboard to improve soldering quality and maintenance convenience.

6.3. Top and Bottom Views

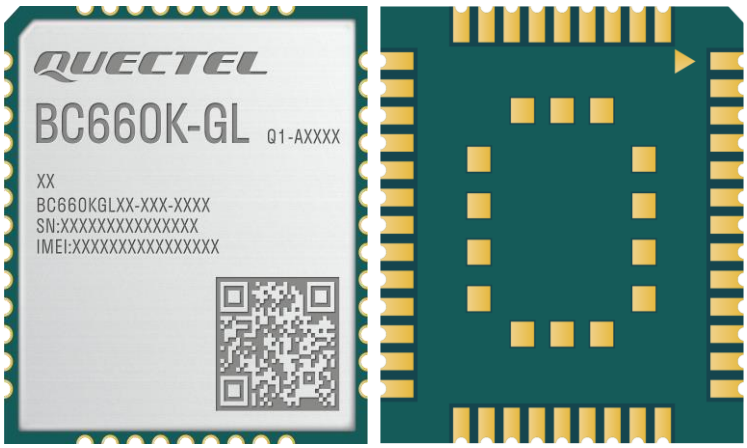


Figure 31: Top and Bottom Views of the Module

NOTE

Images above are for illustration purpose only and may differ from the actual module. For authentic appearance and label, please refer to the module received from Quectel.

7 Storage, Manufacturing and Packaging

7.1. Storage Conditions

The module is provided with vacuum-sealed packaging. MSL of the module is rated as 3. The storage requirements are shown below.

1. Recommended Storage Condition: the temperature should be 23 ±5 °C and the relative humidity should be 35–60 %.

2. Shelf life (in a vacuum-sealed packaging): 12 months in Recommended Storage Condition.

3. Floor life: 168 hours [10] in a factory where the temperature is 23 ±5 °C and relative humidity is below 60 %. After the vacuum-sealed packaging is removed, the module must be processed in reflow soldering or other high-temperature operations within 168 hours. Otherwise, the module should be stored in an environment where the relative humidity is less than 10 % (e.g., a dry cabinet).

4. The module should be pre-baked to avoid blistering, cracks and inner-layer separation in PCB under the following circumstances:

   - The module is not stored in Recommended Storage Condition;
   - Violation of the third requirement mentioned above;
   - Vacuum-sealed packaging is broken, or the packaging has been removed for over 24 hours;
   - Before module repairing.

5. If needed, the pre-baking should follow the requirements below:

   - The module should be baked for 8 hours at 120 ±5 °C;
   - The module must be soldered to PCB within 24 hours after the baking, otherwise it should be put in a dry environment such as in a dry cabinet.

[10] This floor life is only applicable when the environment conforms to *IPC/JEDEC J-STD-033*. It is recommended to start the solder reflow process within 24 hours after the package is removed if the temperature and moisture do not conform to, or are not sure to conform to *IPC/JEDEC J-STD-033*. Do not unpack the modules in large quantities until they are ready for soldering.

NOTE

1. To avoid blistering, layer separation and other soldering issues, extended exposure of the module to the air is forbidden.
2. Take out the module from the package and put it on high-temperature-resistant fixtures before baking. If shorter baking time is desired, see *IPC/JEDEC J-STD-033* for the baking procedure.
3. Pay attention to ESD protection, such as wearing anti-static gloves, when touching the modules.

7.2. Manufacturing and Soldering

Push the squeegee to apply the solder paste on the surface of stencil, thus making the paste fill the stencil openings and then penetrate to the PCB. Apply proper force on the squeegee to produce a clean stencil surface on a single pass. To guarantee module soldering quality, the thickness of stencil for the module is recommended to be 0.15–0.18 mm. For more details, see ***document [5]***.

The recommended peak reflow temperature should be 235–246 ºC, with 246 ºC as the absolute maximum reflow temperature. To avoid damage to the module caused by repeated heating, it is recommended that the module should be mounted only after reflow soldering for the other side of PCB has been completed. The recommended reflow soldering thermal profile (lead-free reflow soldering) and related parameters are shown below.

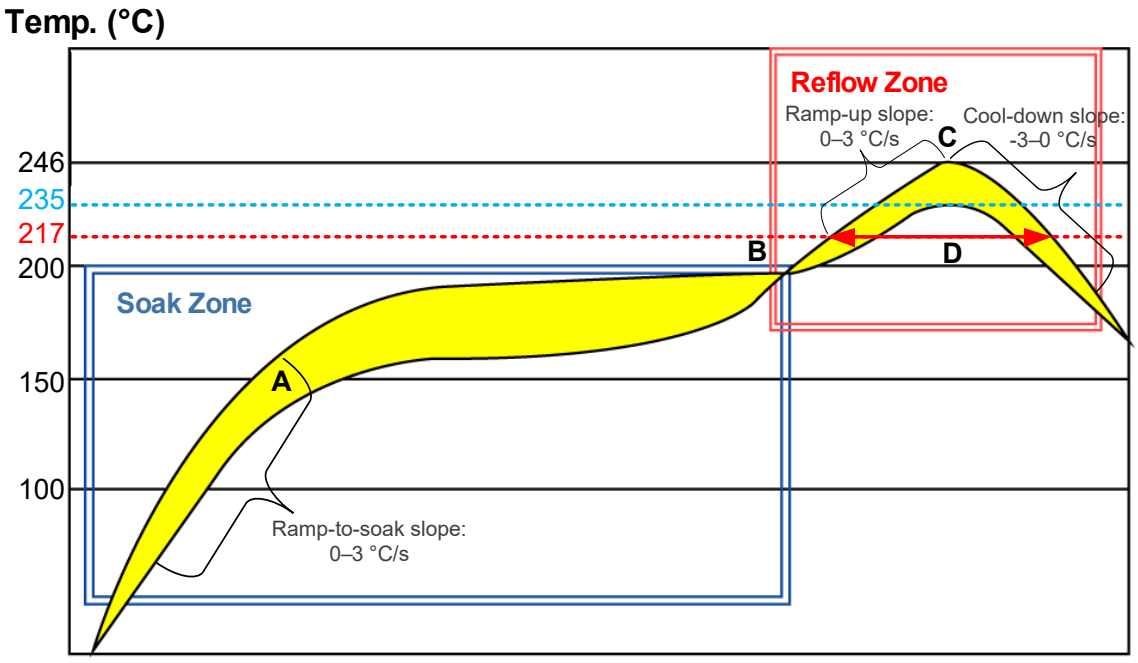


Figure 32: Recommended Reflow Soldering Thermal Profile

Table 34: Recommended Thermal Profile Parameters

Factor	Recommended Value
Soak Zone	
Ramp-to-soak slope	0–3 °C/s
Soak time (between A and B: 150 °C and 200 °C)	70–120 s
Reflow Zone	
Ramp-up slope	0–3 °C/s
Reflow time (D: over 217°C)	40–70 s
Max. temperature	235–246 °C
Cool-down slope	-3–0 °C/s
Reflow Cycle	
Max. reflow cycle	1

NOTE

1. The above profile parameter requirements are for the measured temperature of the solder joints. Both the hottest and coldest spots of solder joints on the PCB should meet the above requirements.
2. During manufacturing and soldering, or any other processes that may contact the module directly, NEVER wipe the module's shielding can with organic solvents, such as acetone, ethyl alcohol, isopropyl alcohol, trichloroethylene, etc. Otherwise, the shielding can may become rusted.
3. The shielding can for the module is made of Cupro-Nickel base material. It is tested that after 12 hours' Neutral Salt Spray test, the laser engraved label information on the shielding can is still clearly identifiable and the QR code is still readable, although white rust may be found.
4. If a conformal coating is necessary for the module, do NOT use any coating material that may chemically react with the PCB or shielding cover, and prevent the coating material from flowing into the module.
5. Avoid using ultrasonic technology for module cleaning since it can damage crystals inside the module.
6. Due to the complexity of the SMT process, please contact Quectel Technical Support in advance for any situation that you are not sure about, or any process (e.g. selective soldering, ultrasonic soldering) that is not mentioned in ***document [5]***.

7.3. Packaging Specification

This chapter describes only the key parameters and process of packaging. All figures below are for reference only. The appearance and structure of the packaging materials are subject to the actual delivery.

The module adopts carrier tape packaging and details are as follow:

7.3.1. Carrier Tape

Dimension details are as follow:

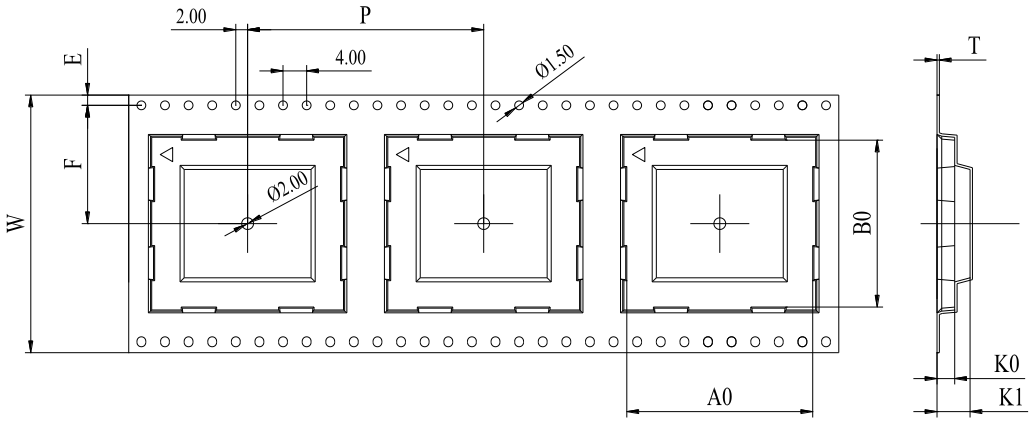


Figure 33: Carrier Tape Dimension Drawing

Table 35: Carrier Tape Dimension Table (Unit: mm)

W	P	T	A0	B0	K0	K1	F	E
32	24	0.4	16.2	18.1	2.8	7.6	14.2	1.75

7.3.2. Plastic Reel

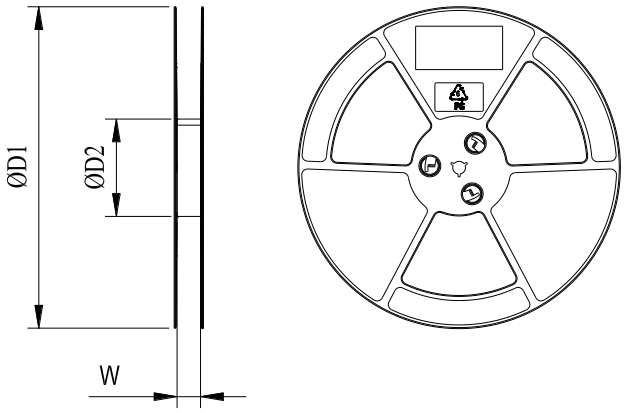


Figure 34: Plastic Reel Dimension Drawing

Table 36: Plastic Reel Dimension Table (Unit: mm)

øD1	øD2	W
330	100	32.5

7.3.3. Mounting Direction

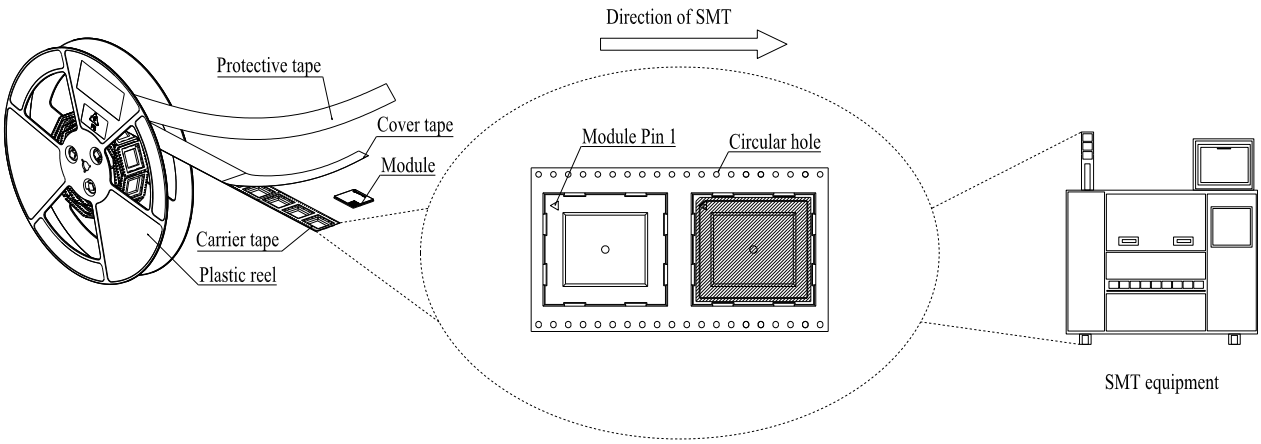
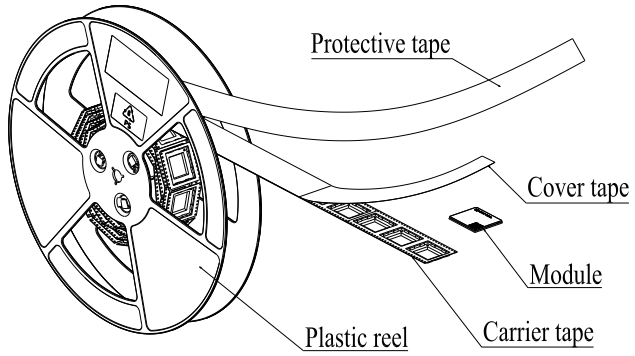


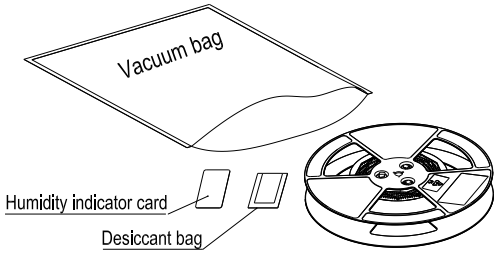
Figure 35: Mounting Direction

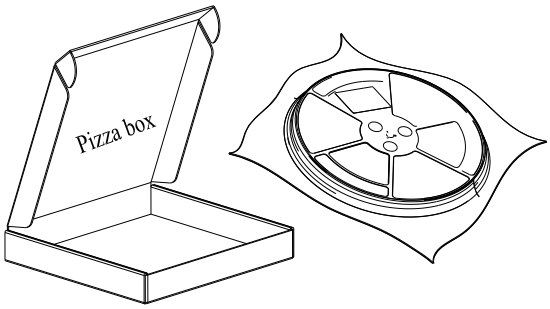
7.3.4. Packaging Process



Place the module into the carrier tape and use the cover tape to cover it; then wind the heat-sealed carrier tape to the plastic reel and use the protective tape for protection. 1 plastic reel can load 250 modules.

Place the packaged plastic reel, 1 humidity indicator card and 1 desiccant bag into a vacuum bag, vacuumize it.





Place the vacuum-packed plastic reel into a pizza box.

Put 4 packaged pizza boxes into 1 carton box and seal it. 1 carton box can pack 1000 modules.

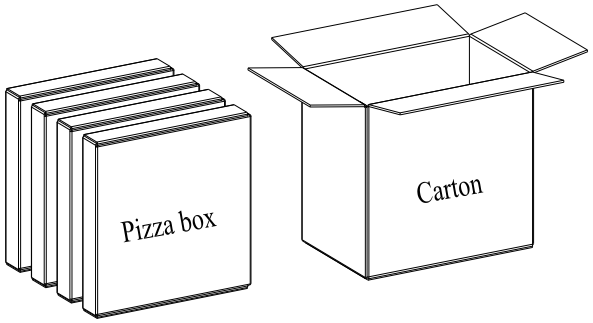


Figure 36: **Packaging Process**

8 Appendix References

Table 37: Related Documents

Document Name
[1] Quectel_BC660K-GL-TE-B_User_Guide
[2] Quectel_BC660K-GL_AT_Commands_Manual
[3] Quectel_BC660K-GL_Reference_Design
[4] Quectel_RF_Layout_Application_Note
[5] Quectel_Module_SMT_Application_Note

Table 38: Terms and Abbreviations

Abbreviation	Description
ADC	Analog-to-Digital Converter
AP	Application Processor
CPU	Central Processing Unit
DRX	Discontinuous Reception
DTLS	Datagram Transport Layer Security
ECL	Enhanced Coverage Level
eDRX	extended Discontinuous Reception
EMI	Electromagnetic Interference
ESD	Electrostatic Discharge
ESR	Equivalent Series Resistance

HD-FDD	Half Frequency Division Duplexing
HTTP	Hyper Text Transfer Protocol
HTTPS	Hyper Text Transfer Protocol over Secure Socket Layer
I/O	Input/Output
I_{PP}	Peak Pulse Current
I_{BR}	Breakdown Current
kbps	Kilobits per second
LCC	Leadless Chip Carrier (package)
LDO	Low-dropout Regulator
LED	Light Emitting Diode
LGA	Land Grid Array
LTE	Long Term Evolution
LwM2M	Lightweight M2M
MSL	Moisture Sensitivity Levels
MQTT	Message Queuing Telemetry Transport
NB-IoT	Narrow Band-Internet of Things
OC	Open Collector
OD	Open Drain
PC	Personal Computer
PCB	Printed Circuit Board
PDN	Public Data Network
PMU	Power Management Unit
PSM	Power Save Mode
PTW	Paging Time Window
RF	Radio Frequency

RTC	Real Time Clock
RXD	Receive Data
SMD	Surface Mount Device
SMS	Short Message Service
TAU	Tracking Area Update
TCP	Transmission Control Protocol
TE	Terminal Equipment
TLS	Transport Layer Security
TXD	Transmitting Data
UART	Universal Asynchronous Receiver & Transmitter
UDP	User Datagram Protocol
UE	User Equipment
URC	Unsolicited Result Code
(U)SIM	Universal Subscriber Identification Module
VSWR	Voltage Standing Wave Ratio
V_{ESD}	Electrostatic Discharge Voltage
Vmax	Maximum Voltage
Vnom	Nominal Voltage
Vmin	Minimum Voltage
V_{IH}max	Maximum High-level Input Voltage
V_{IH}min	Minimum High-level Input Voltage
V_{IL}max	Maximum Low-level Input Voltage
V_{IL}min	Minimum Low-level Input Voltage
$V_I$max	Absolute Maximum Input Voltage
$V_I$nom	Absolute Nominal Input Voltage

$V_I$min	Absolute Minimum Input Voltage
V_{OH}max	Maximum High-level Output Voltage
V_{OH}min	Minimum High-level Output Voltage
V_{OL}max	Maximum Low-level Output Voltage
V_{OL}min	Minimum Low-level Output Voltage
V_{RWM}	Working Peak Reverse Voltage