

The GigaTech Products **QSFP-40G-SR4-GT** is programmed to be fully compatible and functional with all intended CISCO switching devices. This QSFP+ optical transceiver is a parallel fiber optical module with four independent optical transmit and receive channels and is compliant with SFF-8436 and QSFP+ MSA standards. This module is designed for multimode fiber using MPO/MTP connection and operates at a nominal wavelength of 850nm up to 100m over OM3 and 150m over OM4 fiber.

Features:

- Up to 41.2 Gb/s aggregate bit rates
- Four parallel lane design
- Hot-pluggable QSFP+ footprint
- Uncooled 4x10Gb/s 850nm transmitter
- MPO/MTP connector
- Built-in digital diagnostic function
- Up to 100m over OM3, 150m over OM4 fiber
- Single power supply under 1.5W
- Operating temperature range
C-Temp: 0°C to 70°C



Compliance:

- QSFP+ MSA
- MSA SFF-8436
- IEEE 802.3ba
- RoHS Compliant

Applications:

- 40GBASE-SR4 Ethernet
- Breakout to 4X 10GBASE-SR Ethernet
- Infiniband SDR, DDR and QDR

Warranty:

GigaTech Branded Optical Transceivers- Lifetime Warranty

General Specifications - Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Storage Temperature	T_{STO}	-40		100	°C	Ambient Temperature
Bit Error Rate	BER			10^{-12}		
Input Voltage	V_{CC}	3.13	3.3	3.46	V	
Maximum Voltage	V_{MAX}	-0.5		3.6	V	Electrical Power Interface

Link Distances

Parameter	Fiber Type	Modal Bandwidth @ 850nm (MHz-km)	Distance Range (m)
41.2 GBd	50/125um MMF	500 (OM2)	30
	50/125um MMF	2000 (OM3)	100
	50/125um MMF	4700 (OM4)	150 (engineered link)

Optical Characteristics - Transmitter

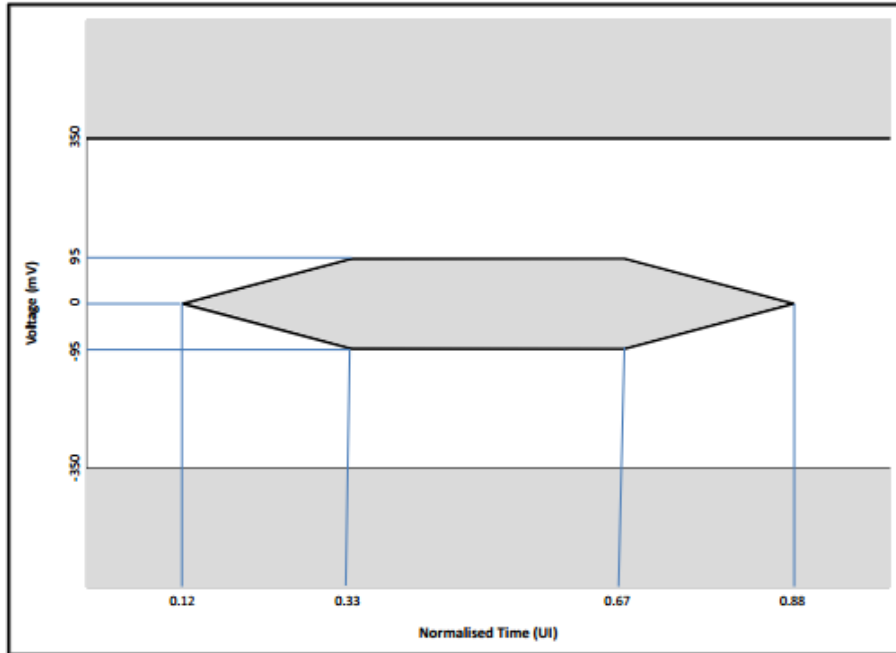
Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Optical Center Wavelength	λ_C	840		860	Nm	
Average Launch Power	P	-7.6		2.4	dBm	Each Lane
Extinction Ratio	ER	3			dB	
RMS Spectral Width (-20 dB)	$\Delta\lambda$			0.65	nm	EIA/TIA-455-127
Relative Intensity Noise (OMA)	RIN			-128	dB/Hz	
Transmit Dispersion Penalty	TDP			3.5	dB	
Launch Power of OFF Transmit	P_{OUT_OFF}			-30	dBm	Average
Optical Eye Mask	Compliant to IEEE 802.3ba Standard					

Optical Characteristics - Receiver

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Optical Center Wavelength	λ_C	840		860	nm	
Optical Input Power (Per Lane)	P_{IN}	-9.5		2.4	dBm	BER of 10^{-12}
Damage Threshold	P	3.3			dBm	
Receiver Sensitivity (Per Lane)	RX_SEN1			-11.1	dBm	
Stressed Receiver Sensitivity				-7.5	dBm	In OMA Per Lane
Receiver Reflectance	TR_{RX}			-12	dB	
LOS Assert	LOS_A	-25			dBm	
LOS De-Assert	LOS_D			-12	dBm	
LOS Hysteresis		0.5			dB	

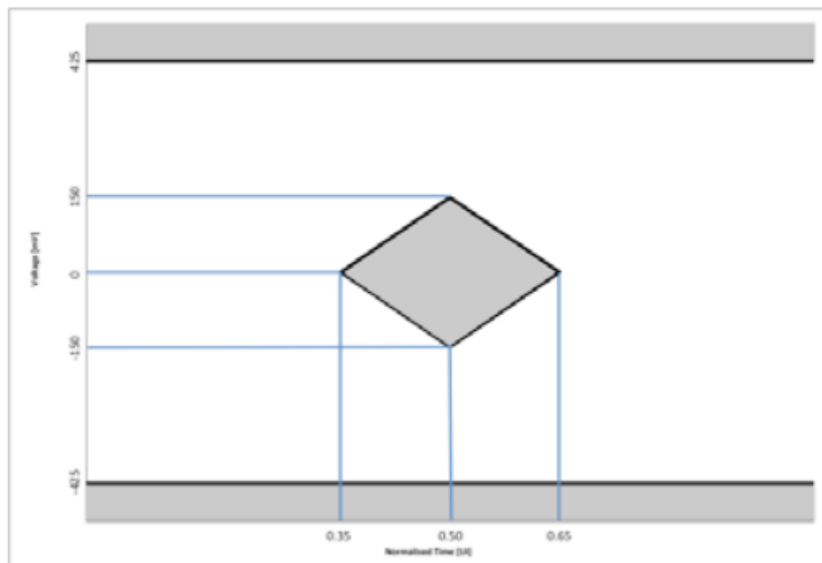
Electrical Characteristics – Transmitter

Parameter	Symbol	Min	Typ	Max	Unit	Remarks
Data Rate Per Channel	DR			10.5	GB/s	Non-Condensing
Differential Input Amplitude	V_{IN_PP}	300		1200	mV	
Transmit Disable Voltage	V_D	$V_{CC}-1.3$		V_{CC}	V	
Transmit Enable Voltage	V_{EN}	V_{EE}		$V_{EE}+0.8$	V	



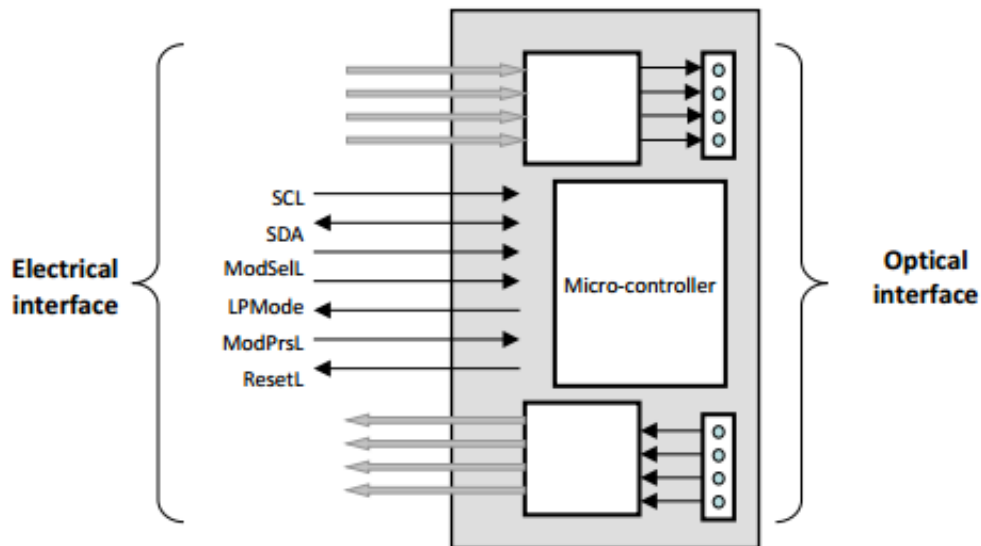
Electrical Characteristics – Receiver

<i>Parameter</i>	<i>Symbol</i>	<i>Min</i>	<i>Typ</i>	<i>Max</i>	<i>Unit</i>	<i>Remarks</i>
Data Rate Per Channel	DR			10.5	GB/s	Non-Condensing
Differential Output Amplitude	V_{OUT_PP}	340		700	mV	
Single Ended Voltage Tolerance	V	-0.3		3.8	V	
Output AC Common Mode Voltage	V_{CM}			7.5	mV	RMS
Output Transition Time	T_R, T_F	28			ps	
Total Jitter	T_J			0.7	Ulp-p	
Deterministic Jitter	DJ			0.4	Ulp-p	



Eye Mask for Hit Ratio = 1×10^{-12}

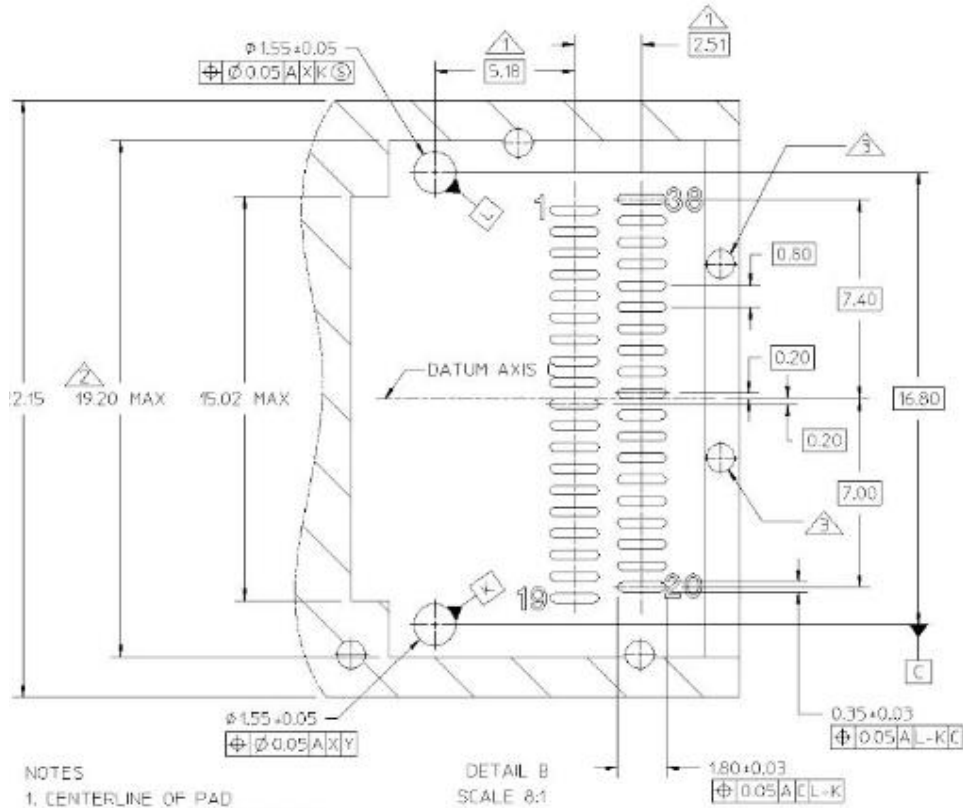
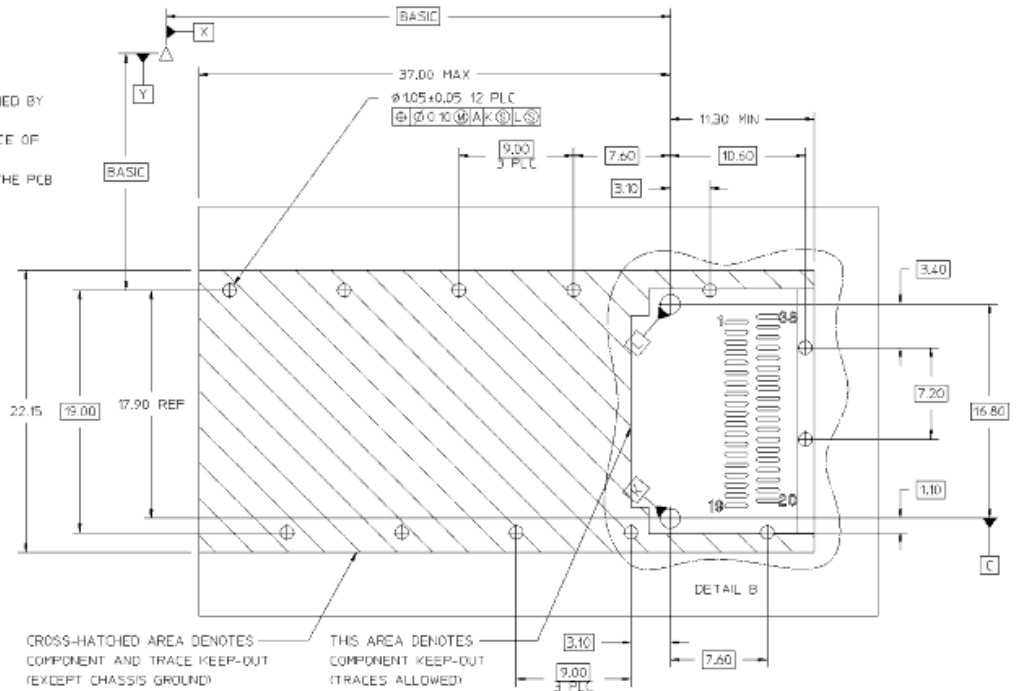
Block Diagram of Transceiver



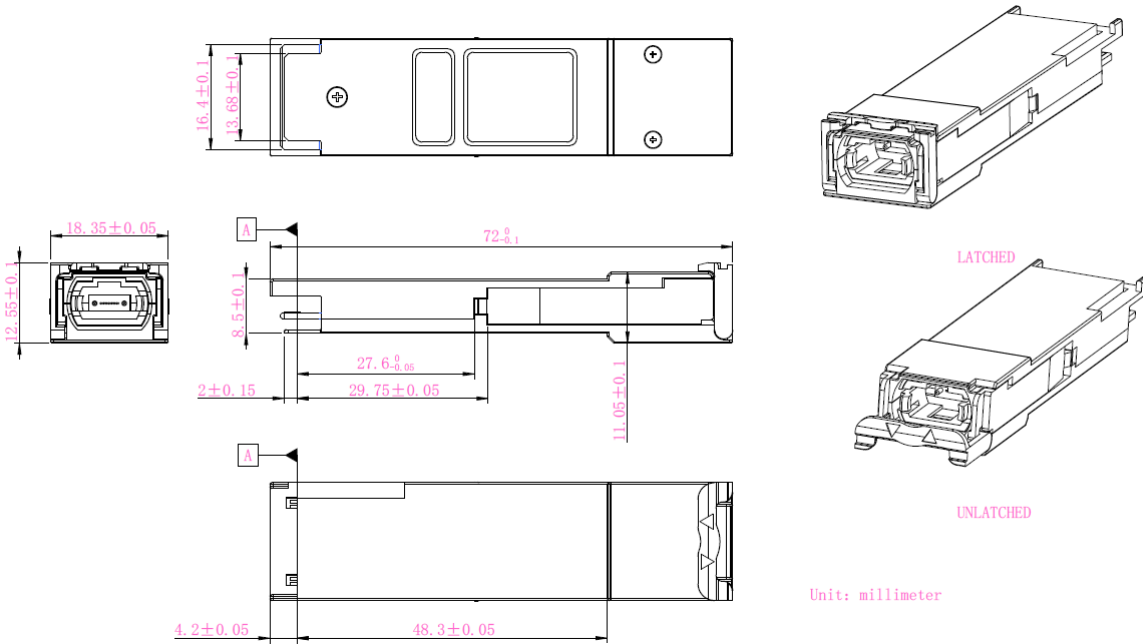
The QSFP-SR4 has a miniature optical engine embedded into the QSFP module. The engine interconnects 4 independent transmit/receive lanes. A functional block diagram of the engine is shown in the above figure. The transmitter section consists of a 4-channel VCSEL array, a 4-channel input buffer and laser driver. An on board micro-controller provides control, diagnostic and monitoring for the cable functions, as well as the external I2C serial communication interface. The Receiver section consists of a 4-channel PIN photodiode array, a 4-channel TIA array, and a 4-channel output buffer.

PCB Layout Recommendation

- NOTES
1. DATUM X & Y ARE ESTABLISHED BY THE CUSTOMER'S FIDUCIAL
 2. DATUM A IS THE TOP SURFACE OF THE HOST BOARD
 3. LOCATION OF THE EDGE OF THE PCB IS APPLICATION SPECIFIC
 4. FINISHED PTH HOLE SIZE

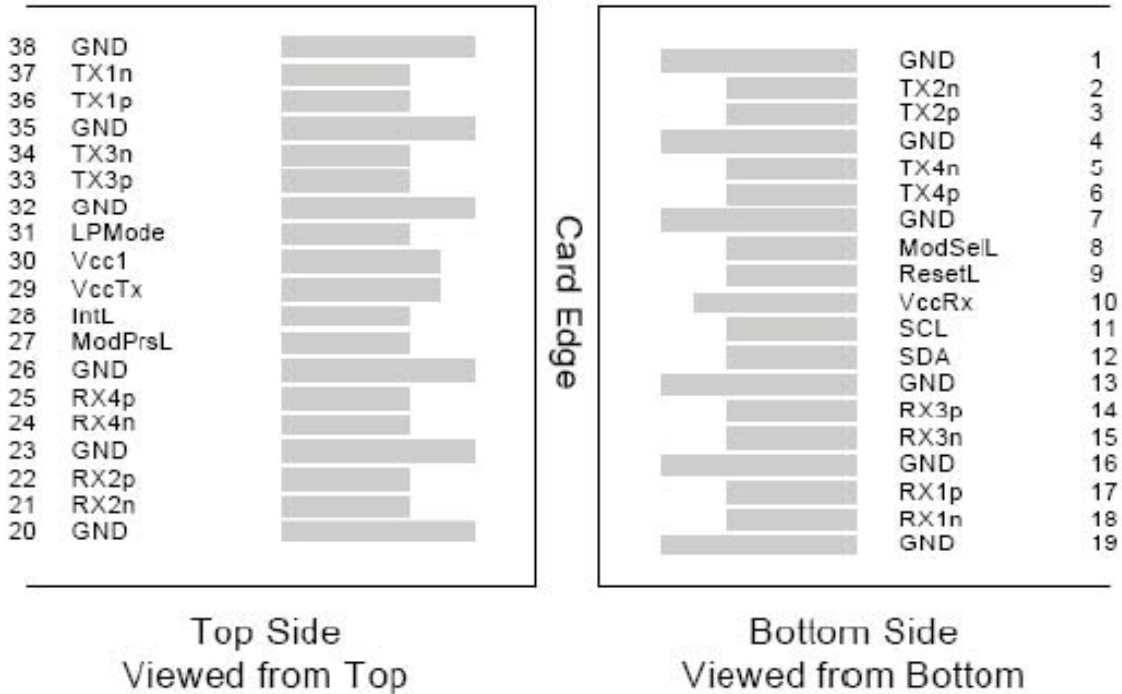


Dimensions



ALL DIMENSIONS ARE ±0.2mm UNLESS OTHERWISE SPECIFIED UNIT: mm

Electrical Pad Layout



Pin Assignment

PIN #	Symbol	Description	Remarks
1	GND	Ground	
2	Tx2n	Transmitter Inverted Data Input	
3	Tx2p	Transmitter Non-Inverted Data Input	
4	GND	Ground	
5	Tx4n	Transmitter Inverted Data Input	
6	Tx4p	Transmitter Non-Inverted Data Input	
7	GND	Ground	
8	ModSelL	Module Select	
9	ResetL	Module Reset	
10	Vcc RX	+3.3V Power Supply Receiver	
11	SCL	2-wire serial interface clock	
12	SDA	2-wire serial interface data	
13	GND	Ground	
14	Rx3p	Receiver Non-Inverted Data Output	
15	Rx3n	Receiver Inverted Data Output	
16	GND	Ground	
17	Rx1p	Receiver Non-Inverted Data Output	
18	Rx1n	Receiver Inverted Data Output	
19	GND	Ground	
20	GND	Ground	
21	Rx2n	Receiver Inverted Data Output	
22	Rx2p	Receiver Non-Inverted Data Output	
23	GND	Ground	
24	Rx4n	Receiver Inverted Data Output	
25	Rx4p	Receiver Non-Inverted Data Output	
26	GND	Ground	
27	ModPrsL	Module Present	
28	IntL	Interrupt	
29	Vcc TX	+3.3V Power Supply transmitter	
30	Vcc1	+3.3V Power Supply	
31	LPMMode	Low Power Mode	
32	GND	Ground	
33	Tx3p	Transmitter Non-Inverted Data Input	
34	Tx3n	Transmitter Inverted Data Input	
35	GND	Ground	
36	Tx1p	Transmitter Non-Inverted Data Input	
37	Tx1n	Transmitter Inverted Data Input	
38	GND	Ground	

References

1. IEEE standard 802.3ba. IEEE Standard Department, 2010.
2. QSFP+ 10Gbs 4X PLUGGABLE TRANSCEIVER – SFF-8436