

Extract of Test report: 28106391 001
“Determination of electrical properties”

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Appendix 4 Type Verification Test Report (G83/2)

Type of System:	Grid tied inverter											
System Manufacturer: Manufacturer data:	Power-One Italy S.p.A. Via S. Giorgio 642, 52028 Terranuova Bracciolini (AR) - Italy											
Reference test report:	28106391 001											
Measuring period:	From 20 Th January 2014 to 14 Th February 2014											
Pacr: (Rated AC Power) Pacmax: (Maximum AC output Power)	<table border="1"> <thead> <tr> <th>Models *</th> <th>Pacr / Pacmax</th> </tr> </thead> <tbody> <tr> <td>PVI-3.6-TL-OUTD</td> <td rowspan="3">3600 W / 3680 W **</td> </tr> <tr> <td>PVI-3.6-TL-OUTD-S</td> </tr> <tr> <td>PVI-3.6-TL-OUTD-W</td> </tr> <tr> <td>PVI-3.0-TL-OUTD</td> <td rowspan="3">3000 W / 3300 W</td> </tr> <tr> <td>PVI-3.0-TL-OUTD-S</td> </tr> <tr> <td>PVI-3.0-TL-OUTD-W</td> </tr> </tbody> </table>		Models *	Pacr / Pacmax	PVI-3.6-TL-OUTD	3600 W / 3680 W **	PVI-3.6-TL-OUTD-S	PVI-3.6-TL-OUTD-W	PVI-3.0-TL-OUTD	3000 W / 3300 W	PVI-3.0-TL-OUTD-S	PVI-3.0-TL-OUTD-W
Models *	Pacr / Pacmax											
PVI-3.6-TL-OUTD	3600 W / 3680 W **											
PVI-3.6-TL-OUTD-S												
PVI-3.6-TL-OUTD-W												
PVI-3.0-TL-OUTD	3000 W / 3300 W											
PVI-3.0-TL-OUTD-S												
PVI-3.0-TL-OUTD-W												
Software version	<table border="1"> <tbody> <tr> <td>Booster (DC-DC)</td> <td>Higher than A.3.3.6</td> </tr> <tr> <td>Inverter (DC-AC)</td> <td>Higher than B.3.4.B</td> </tr> <tr> <td>MICRO (Supervisor)</td> <td>Higher than C.0.3.5</td> </tr> </tbody> </table>		Booster (DC-DC)	Higher than A.3.3.6	Inverter (DC-AC)	Higher than B.3.4.B	MICRO (Supervisor)	Higher than C.0.3.5				
Booster (DC-DC)	Higher than A.3.3.6											
Inverter (DC-AC)	Higher than B.3.4.B											
MICRO (Supervisor)	Higher than C.0.3.5											
Rated Voltage:	2-phase devices 230 V (Phase/ Neutral)											
<p>Remarks:</p> <p>Note *: test performed on model PVI-3.6-TL-OUTD and PVI-3.0-TL-OUTD The test result found can be extended on all model of the same product family. All products are completely the same; identical software version and PCB control boards are installed; the difference is related only on output power set.</p> <p>The family product model is made by the following products: PVI-3.6-TL-OUTD-W ; PVI-3.6-TL-OUTD-S PVI-3.0-TL-OUTD-W ; PVI-3.0-TL-OUTD-S</p> <p>Tested model indicated in bold characters.</p> <p>Note **: Maximum output current limited to 16A up to a maximum output power of 3.68kW</p>												

Power Quality. Harmonics. The requirement is specified in section 5.4.1, test procedure in Annex A or B 1.4.1 (of reference document G83/2)						
MODELS: PVI-3.6-TL-OUTD ; PVI-3.6-TL-OUTD-S ; PVI-3.6-TL-OUTD-W						
SSEG rating per phase (rpp)			3,6	kW	NV=MV*3.68/rpp	
Harmonic	At 45-55% of rated output		100% of rated output		Limit in BS EN 61000-3-2 in Amps	Higher limit for odd harmonics 21 and above
	Measured Value (MV) in Amps	Normalised Value (NV) in Amps	Measured Value (MV) in Amps	Normalised Value (NV) in Amps		
2	0,021	0,021	0,031	0,032	1,080	
3	0,186	0,190	0,258	0,264	2,300	
4	0,007	0,007	0,011	0,011	0,430	
5	0,053	0,054	0,033	0,034	1,140	
6	0,006	0,006	0,003	0,003	0,300	
7	0,046	0,047	0,057	0,058	0,770	
8	0,005	0,005	0,008	0,008	0,230	
9	0,049	0,050	0,041	0,042	0,400	
10	0,004	0,004	0,006	0,006	0,184	
11	0,044	0,045	0,044	0,045	0,330	
12	0,006	0,006	0,006	0,006	0,153	
13	0,039	0,040	0,050	0,051	0,210	
14	0,005	0,005	0,006	0,006	0,131	
15	0,027	0,028	0,037	0,038	0,150	
16	0,004	0,004	0,003	0,003	0,115	
17	0,021	0,021	0,040	0,041	0,132	
18	0,003	0,003	0,005	0,005	0,102	
19	0,014	0,014	0,035	0,036	0,118	
20	0,003	0,003	0,005	0,005	0,092	
21	0,010	0,010	0,031	0,032	0,107	
22	0,004	0,004	0,003	0,003	0,084	
23	0,004	0,004	0,025	0,026	0,098	0,147
24	0,003	0,003	0,003	0,003	0,077	
25	0,003	0,003	0,017	0,017	0,090	0,135
26	0,003	0,003	0,004	0,004	0,071	
27	0,002	0,002	0,015	0,015	0,083	0,124
28	0,003	0,003	0,004	0,004	0,066	
29	0,005	0,005	0,010	0,010	0,078	0,117
30	0,004	0,004	0,003	0,003	0,061	

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31	0,004	0,004	0,011	0,011	0,073	0,109
32	0,003	0,003	0,003	0,003	0,058	
33	0,003	0,003	0,005	0,005	0,068	0,102
34	0,004	0,004	0,004	0,004	0,054	
35	0,003	0,003	0,005	0,005	0,064	0,096
36	0,002	0,002	0,003	0,003	0,051	
37	0,004	0,004	0,005	0,005	0,061	0,091
38	0,003	0,003	0,002	0,002	0,048	
39	0,004	0,004	0,003	0,003	0,058	0,087
40	0,003	0,003	0,003	0,003	0,046	

No Higher limit for odd harmonics 21 and above are applied

Power Quality. Harmonics. The requirement is specified in section 5.4.1, test procedure in Annex A or B 1.4.1 (of reference document G83/2)

MODELS: PVI-3.0-TL-OUTD ; PVI-3.0-TL-OUTD-S ; PVI-3.0-TL-OUTD-W

SSEG rating per phase (rpp)		3,0	kW		NV=MV*3.68/rpp	
Harmonic	At 45-55% of rated output	100% of rated output				
	Measured Value (MV) in Amps	Normalised Value (NV) in Amps	Measured Value (MV) in Amps	Normalised Value (NV) in Amps	Limit in BS EN 61000-3- 2 in Amps	Higher limit for odd harmonics 21 and above
2	0,015	0,018	0,020	0,025	1,080	
3	0,228	0,280	0,445	0,546	2,300	
4	0,005	0,006	0,005	0,006	0,430	
5	0,059	0,072	0,075	0,092	1,140	
6	0,005	0,006	0,003	0,004	0,300	
7	0,053	0,065	0,064	0,079	0,770	
8	0,006	0,007	0,005	0,006	0,230	
9	0,045	0,055	0,054	0,066	0,400	
10	0,003	0,004	0,005	0,006	0,184	
11	0,036	0,044	0,045	0,055	0,330	
12	0,006	0,007	0,006	0,007	0,153	
13	0,028	0,034	0,042	0,052	0,210	
14	0,004	0,005	0,005	0,006	0,131	
15	0,021	0,026	0,042	0,052	0,150	
16	0,004	0,005	0,007	0,009	0,115	
17	0,017	0,021	0,044	0,054	0,132	
18	0,003	0,004	0,004	0,005	0,102	
19	0,006	0,007	0,033	0,040	0,118	

20	0,002	0,002	0,004	0,005	0,092	
21	0,004	0,005	0,025	0,031	0,107	
22	0,002	0,002	0,004	0,005	0,084	
23	0,003	0,004	0,015	0,018	0,098	0,147
24	0,004	0,005	0,003	0,004	0,077	
25	0,003	0,004	0,014	0,017	0,090	0,135
26	0,003	0,004	0,003	0,004	0,071	
27	0,004	0,005	0,006	0,007	0,083	0,124
28	0,003	0,004	0,001	0,001	0,066	
29	0,005	0,006	0,003	0,004	0,078	0,117
30	0,003	0,004	0,004	0,005	0,061	
31	0,003	0,004	0,005	0,006	0,073	0,109
32	0,002	0,002	0,003	0,004	0,058	
33	0,003	0,004	0,004	0,005	0,068	0,102
34	0,004	0,005	0,002	0,002	0,054	
35	0,002	0,002	0,004	0,005	0,064	0,096
36	0,003	0,004	0,004	0,005	0,051	
37	0,002	0,002	0,002	0,002	0,061	0,091
38	0,002	0,002	0,002	0,002	0,048	
39	0,001	0,001	0,005	0,006	0,058	0,087
40	0,003	0,004	0,003	0,004	0,046	

No Higher limit for odd harmonics 21 and above are applied

Power Quality. Voltage fluctuations and Flicker. The requirement is specified in section 5.4.2, test procedure in Annex A or B 1.4.3 (of reference document G83/2)

 MODELS: **PVI-3.6-TL-OUTD** ; PVI-3.6-TL-OUTD-S ; PVI-3.6-TL-OUTD-W
 PVI-3.0-TL-OUTD ; PVI-3.0-TL-OUTD-S ; PVI-3.0-TL-OUTD-W

	Starting			Stopping			Running	
	dmax	dc	d(t)	dmax	dc	d(t)	Pst	Plt 2 hours
Measured Values	1,004%	0%	0	1,004%	0%	0	0,243	0,242
Normalised to standard impedance and 3.68kW for multiple units	N/A	N/A	N/A	N/A	N/A	N/A	N/A	N/A
Limits set under BS EN 61000-3-3	4%	3,30%	3.3% 500ms	4%	3,30%	3.3% 500ms	1	0,65
Test start date	03\10\2011			Test end date			03\10\2011	

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Power quality. DC injection. The requirement is specified in section 5.5, test procedure in Annex A or B 1.4.4 (of reference document G83/2)

MODELS: PVI-3.6-TL-OUTD ; PVI-3.6-TL-OUTD-S ; PVI-3.6-TL-OUTD-W			
Test power level	10%	55%	100%
Recorded value	3,0 mA	2,0 mA	3,0 mA
as % of rated AC current	0,02 %	0,01 %	0,02 %
Limit	0,25 %	0,25 %	0,25 %
MODELS: PVI-3.0-TL-OUTD ; PVI-3.0-TL-OUTD-S ; PVI-3.0-TL-OUTD-W			
Test power level	10%	55%	100%
Recorded value(A)	1,92 mA	1,46 mA	5,12 mA
as % of rated AC current	0,02%	0,01%	0,04%
Limit	0,25%	0,25%	0,25%

Power quality. DC injection. The requirement is specified in section 5.6, test procedure in Annex A or B 1.4.2 (of reference document G83/2)

MODELS: PVI-3.6-TL-OUTD ; PVI-3.6-TL-OUTD-S ; PVI-3.6-TL-OUTD-W				
	216.2V	230V	253V	Measured at three voltage levels and at full output. Voltage to be maintained within $\pm 1.5\%$ of the stated level during the test.
Measured value	0,9994	0,9994	0,9994	
Limit	>0.95	>0.95	>0.95	
MODELS: PVI-3.0-TL-OUTD ; PVI-3.0-TL-OUTD-S ; PVI-3.0-TL-OUTD-W				
	216.2V	230V	253V	Measured at three voltage levels and at full output. Voltage to be maintained within $\pm 1.5\%$ of the stated level during the test.
Measured value	0,9988	0,9986	0,9988	
Limit	>0.95	>0.95	>0.95	

Protection. Frequency tests The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.3 (of reference document G83/2)

 MODELS: **PVI-3.6-TL-OUTD** ; PVI-3.6-TL-OUTD-S ; PVI-3.6-TL-OUTD-W

Function	Setting		Trip test		“No trip tests”	
	Frequency	Time delay	Frequency	Time delay	Frequency /time	Confirm no trip
U/F stage 1	47.5Hz	20,05s	47,45	20,04	47.7Hz/ 25s	No Trip
U/F stage 2	47Hz	0,55s	46,95	0,56	47.2Hz/ 19.98s	No Trip
					46.8Hz/ 0.48s	No Trip
O/F stage 1	51.5Hz	90,05s	51,55	90,04	51.3Hz/95s	No Trip
O/F stage 2	52Hz	0,55s	52,05	0,55	51.8Hz/ 89.98s	No Trip
					52.2Hz/ 0.48s	No Trip

 MODELS: **PVI-3.0-TL-OUTD** ; PVI-3.0-TL-OUTD-S ; PVI-3.0-TL-OUTD-W

Function	Setting		Trip test		“No trip tests”	
	Frequency	Time delay	Frequency	Time delay	Frequency /time	Confirm no trip
U/F stage 1	47.5Hz	20,05s	47,45	20,03	47.7Hz/ 25s	No Trip
U/F stage 2	47Hz	0,55s	46,95	0,55	47.2Hz/ 19.98s	No Trip
					46.8Hz/ 0.48s	No Trip
O/F stage 1	51.5Hz	90,05s	51,55	90,03	51.3Hz/ 95s	No Trip
O/F stage 2	52Hz	0,55s	52,05	0,55	51.8Hz/ 89.98s	No Trip
					52.2Hz/ 0.48s	No Trip

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Protection. Voltage tests The requirement is specified in section 5.3.1, test procedure in Annex A or B 1.3.2 (of reference document G83/2)

MODELS: **PVI-3.6-TL-OUTD** ; PVI-3.6-TL-OUTD-S ; PVI-3.6-TL-OUTD-W

Function	Setting		Trip test		“No trip tests”	
	Voltage	Time delay	Voltage	Time delay	Voltage/Time	Confirm no trip
U/V stage 1	200.1V	2.55s	199,93	2,59	204.1V/3.5s	No Trip
U/V stage 2	184V	0.55s	184,06	0,60	188V/2.48s	No Trip
					180V/0.48s	No Trip
O/V stage 1	262.2V	1.05s	261,90	1,07	258.2V/2.0s	No Trip
O/V stage 2	273.7V	0.55s	273,18	0,59	269.7V/0.98s	No Trip
					277.7V/ 0.48s	No Trip

MODELS: **PVI-3.0-TL-OUTD** ; PVI-3.0-TL-OUTD-S ; PVI-3.0-TL-OUTD-W

Function	Setting		Trip test		“No trip tests”	
	Voltage	Time delay	Voltage	Time delay	Voltage/Time	Confirm no trip
U/V stage 1	200.1V	2.55s	199,85	2,57	204.1V/3.5s	No Trip
U/V stage 2	184V	0.55s	183,73	0,588	188V/2.48s	No Trip
					180V/0.48s	No Trip
O/V stage 1	262.2V	1.05s	261,94	1,08	258.2V/2.0s	No Trip
O/V stage 2	273.7V	0.55s	273,32	0,579	269.7V/0.98s	No Trip
					277.7V/ 0.48s	No Trip

Protection. Loss of Mains test. The requirement is specified in section 5.3.2, test procedure in Annex A or B 1.3.4 (of reference document G83/2)

Note as an alternative, inverters can be tested to BS EN 62116. The following sub set of tests should be recorded in the following table.

MODELS: **PVI-3.6-TL-OUTD** ; PVI-3.6-TL-OUTD-S ; PVI-3.6-TL-OUTD-W

Test Power and imbalance	33% -5% Q Test 22	66% 5% Q Test 12	- 100% -5% P Test 5	33% +5% Q Test 31	66% +5% Q Test 21	100% +5% P Test 10
Trip time. Limit is 0.5s	0,264	0,388	0,432	0,345	0,133	0,397

MODELS: **PVI-3.0-TL-OUTD** ; PVI-3.0-TL-OUTD-S ; PVI-3.0-TL-OUTD-W

Test Power and imbalance	33% -5% Q Test 22	66% 5% Q Test 12	- 100% -5% P Test 5	33% +5% Q Test 31	66% +5% Q Test 21	100% +5% P Test 10
Trip time. Limit is 0.5s	0,392	0,362	0,348	0,369	0,376	0,380

Protection. Frequency change, Stability test The requirement is specified in section 5.3.3, test procedure in Annex A or B 1.3.6 (of reference document G83/2)

 MODELS: **PVI-3.6-TL-OUTD** ; PVI-3.6-TL-OUTD-S ; PVI-3.6-TL-OUTD-W

	Start Frequency	Change	End Frequency	Confirm no trip
Positive Vector Shift	49.5Hz	+9 degrees		No trip
Negative Vector Shift	50.5Hz	- 9 degrees		No trip
Positive Frequency drift	49.5Hz	+0.19Hz/sec	51.5Hz	No trip
Negative Frequency drift	50.5Hz	-0.19Hz/sec	47.5Hz	No trip

MODELS: PVI-3.0-TL-OUTD ; PVI-3.0-TL-OUTD-S ; PVI-3.0-TL-OUTD-W				
	Start Frequency	Change	End Frequency	Confirm no trip
Positive Vector Shift	49.5Hz	+9 degrees		No trip
Negative Vector Shift	50.5Hz	- 9 degrees		No trip
Positive Frequency drift	49.5Hz	+0.19Hz/sec	51.5Hz	No trip
Negative Frequency drift	50.5Hz	-0.19Hz/sec	47.5Hz	No trip

Protection. Re-connection timer. The requirement is specified in section 5.3.4, test procedure in Annex A or B 1.3.5 (of reference document G83/2)

 MODELS: **PVI-3.6-TL-OUTD** ; PVI-3.6-TL-OUTD-S ; PVI-3.6-TL-OUTD-W

Time delay setting	Measured delay	Checks on no reconnection when voltage or frequency is brought to just outside stage 1 limits of table 1.			
20s	35s	At 266.2V	At 196.1V	At 47.4Hz	At 51.6Hz
Confirmation that the SSEG does not re-connect.		No reconnection	No reconnection	No reconnection	No reconnection

MODELS: PVI-3.0-TL-OUTD ; PVI-3.0-TL-OUTD-S ; PVI-3.0-TL-OUTD-W					
Time delay setting	Measured delay	Checks on no reconnection when voltage or frequency is brought to just outside stage 1 limits of table 1.			
20s	35s	At 266.2V	At 196.1V	At 47.4Hz	At 51.6Hz
Confirmation that the SSEG does not re-connect.		No reconnection	No reconnection	No reconnection	No reconnection

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Fault level contribution. The requirement is specified in section 5.7, test procedure in Annex A or B 1.4.6 (of reference document G83/2)

MODELS: **PVI-3.6-TL-OUTD** ; PVI-3.6-TL-OUTD-S ; PVI-3.6-TL-OUTD-W

For a Inverter SSEG

Time after fault	Volts	Amps
20ms	101,42	14,16
100ms	94,89	10,33
250ms	93,70	8,30
500ms	93,30	7,41
Time to trip	0,588	In seconds

MODELS: **PVI-3.0-TL-OUTD** ; PVI-3.0-TL-OUTD-S ; PVI-3.0-TL-OUTD-W

For a Inverter SSEG

Time after fault	Volts	Amps
20ms	83,48	14,28
100ms	43,06	8,21
250ms	32,65	5,34
500ms	28,31	3,91
Time to trip	0,582	In seconds

Self-Monitoring solid state switching. The requirement is specified in section 5.3.1, no specified test requirements.

NA

Mechanical relay used.

This extract from the test report is only valid in conjunction with the test report no.: **28106391 001**